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Towards a Model for Impact of Technology Evolution on Wafer-Level ESD Damage Susceptibility

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Setting the Stage

- Wafer level ESD damage has long been a mystery
- Investigators lacked tools to detect events *in situ*
- Often yields were low and any ESD was masked by other handling-induced errors
- Early robotic equipment was more sensitive than the wafers
- Electrostatic attraction (ESA) emerged as the more significant problem
- Some ESA mitigation techniques probably also reduce ESD risk
- ESD vulnerability very dependent on specific wafer construction
- Attitudes range widely from indifference to serious concern
- Little being done, few actual investigations

Some Prior Work

- Early processing at AT&T (1970-1980) – Failures at wafer level a major problem
- Burr Brown (1991 EOS/ESD Symposium) - “streaming potential” causes ESD damage at wafer rinse
- Seagate (1998 EOS/ESD symposium) – Damage to MR Heads at Ion Milling (not really ESD but vulnerabilities may be similar)
- Jacob & Nicoletti (2006 IEEE Trans Dev Mat Rel) – Allude to ESD damage “directly to chip surface”

Some Prior Work

- **Infineon (2006 EOS/ESD Symposium) - claim *no damage* at wafer saw**
- **Infineon 2007 Future-Fab article – On-going efforts to eliminate ESD events driven by fear of device damage but no direct evidence cited**
- **Damage at wafer saw – Direct experience**

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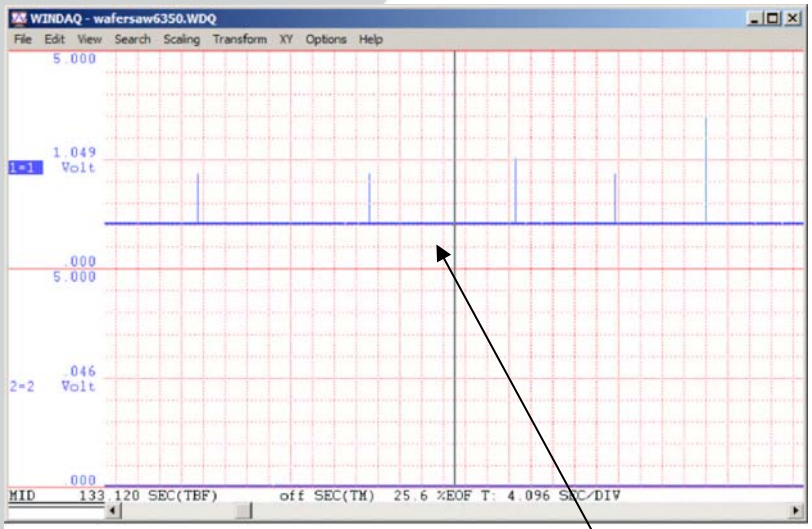
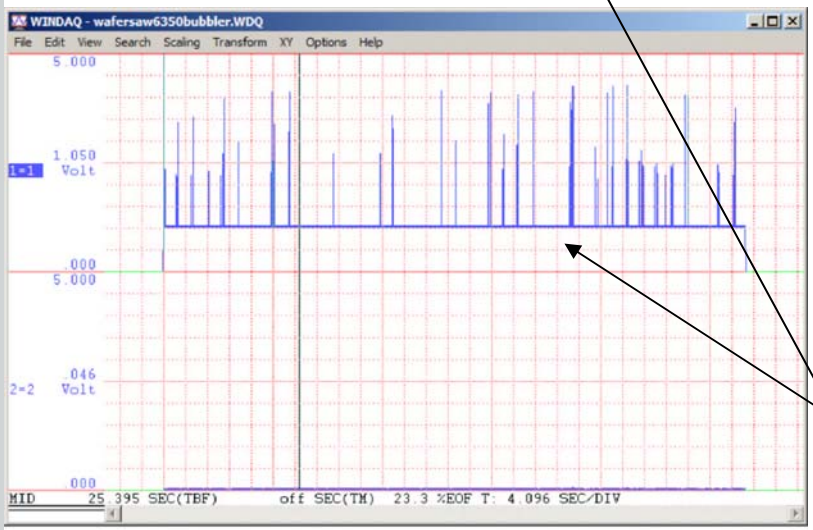
Wafer Saw ESD Events





Wafer Saw 6351 – CO2 bubbler on

Wafer Saw 6351 – CO2 bubbler off

Events captured by ESD event detector

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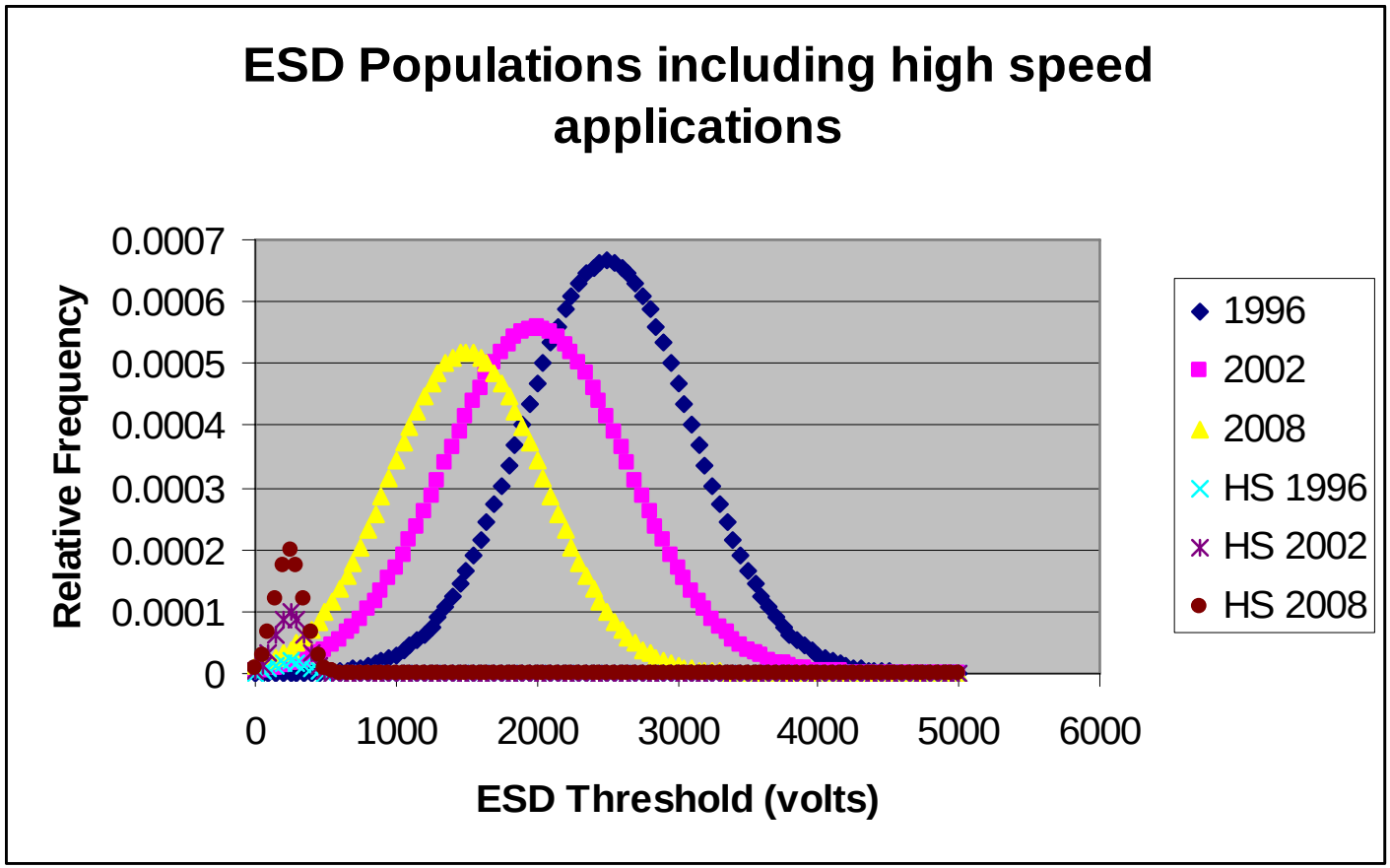
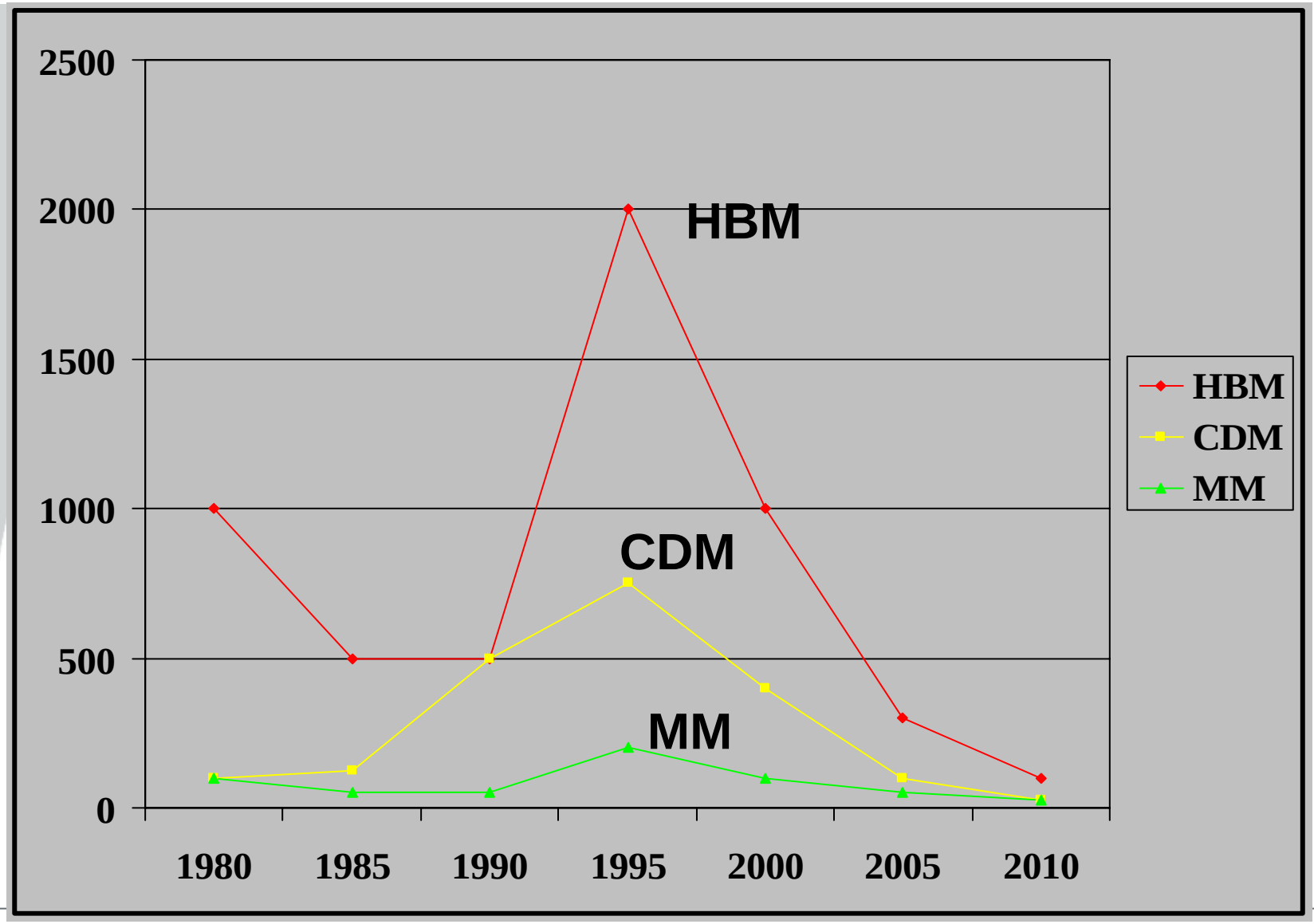
ESD Threshold Populations including high speed applications

Distribution becoming bimodal



ESDA Technology Roadmap



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Wafer Level ESD Model

- Details of the Model
- Results
- Limitations and Improvements

Wafer-Level ESD Model

Objectives

- Create a framework for predicting voltage levels on wafers due to ESD in the front-end environment
- Estimate how geometric changes in wafer construction affect ESD vulnerability
- Identify processing and feature scale information needed to improve estimates

Strategy

- Develop a computer model for typical wafer-level ESD event
- Base model on a charged-device model (CDM) scenario (wafer grounded in a static field)

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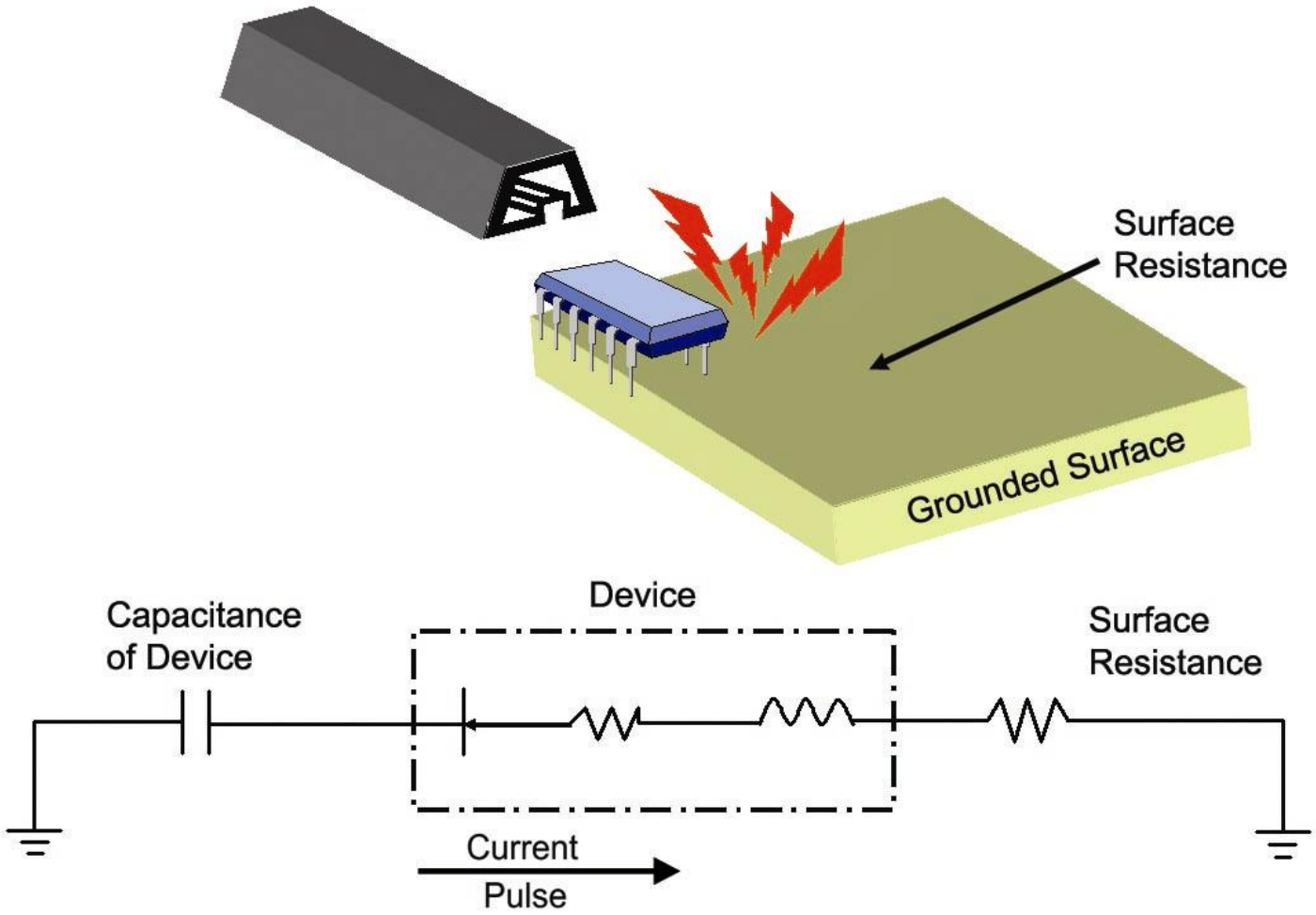
Charged Device Model



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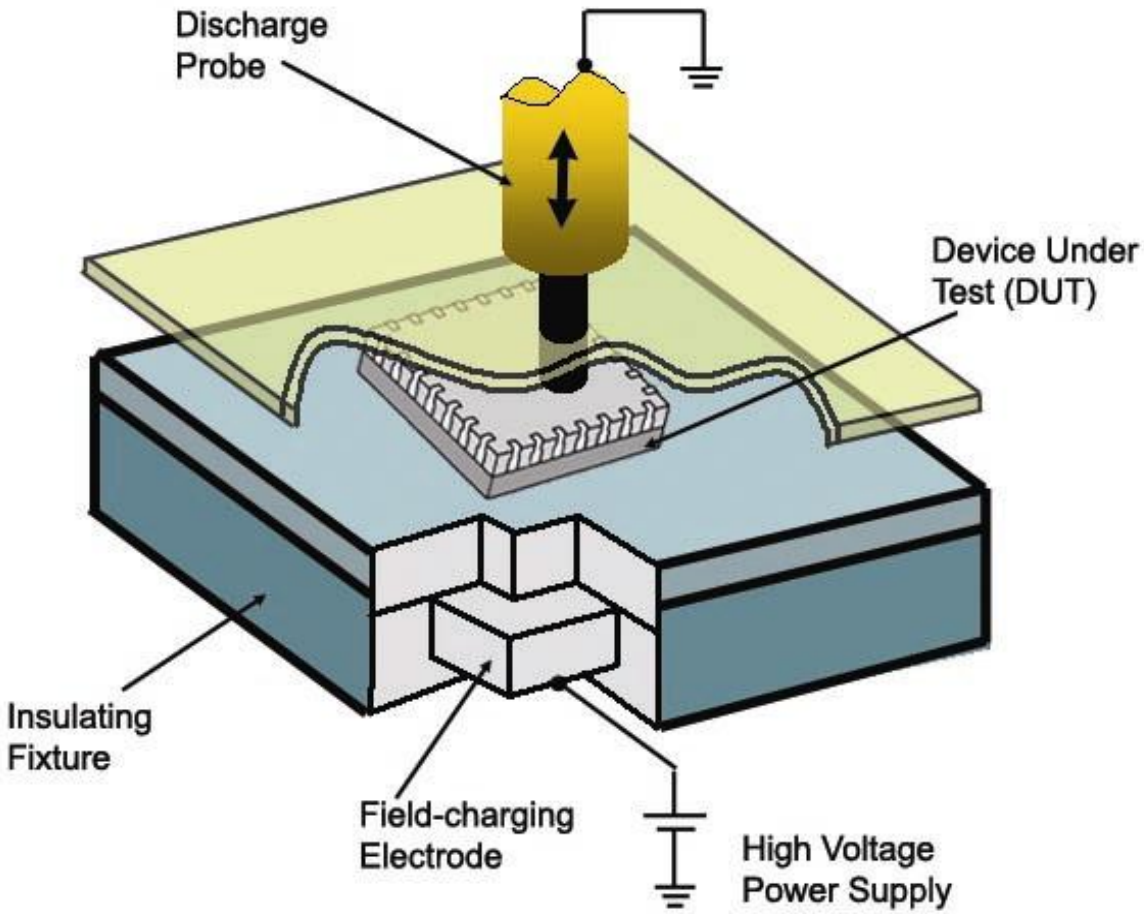
FCDM Simulator



Model Description

- **Integrated Wafer-Simulator CDM Model**
  - Wafer modeled as an array of capacitances with respect to the field source
    - Technology evolution related to this capacitance variation
  - Feature-to-feature and feature-to backside capacitances are small and neglected for this analysis
  - Feature-to-feature potential differences used as an indicator of device failure
  - Thermal effects were not considered since any significant heating would be on back side of wafer well away from sensitive features
  - Changes to new materials (e.g., ZrO_2) are not included
- **The following lumped-elements were used in circuit model for the CDM generator**
  - Nonlinear arc resistance
  - Ground probe inductance

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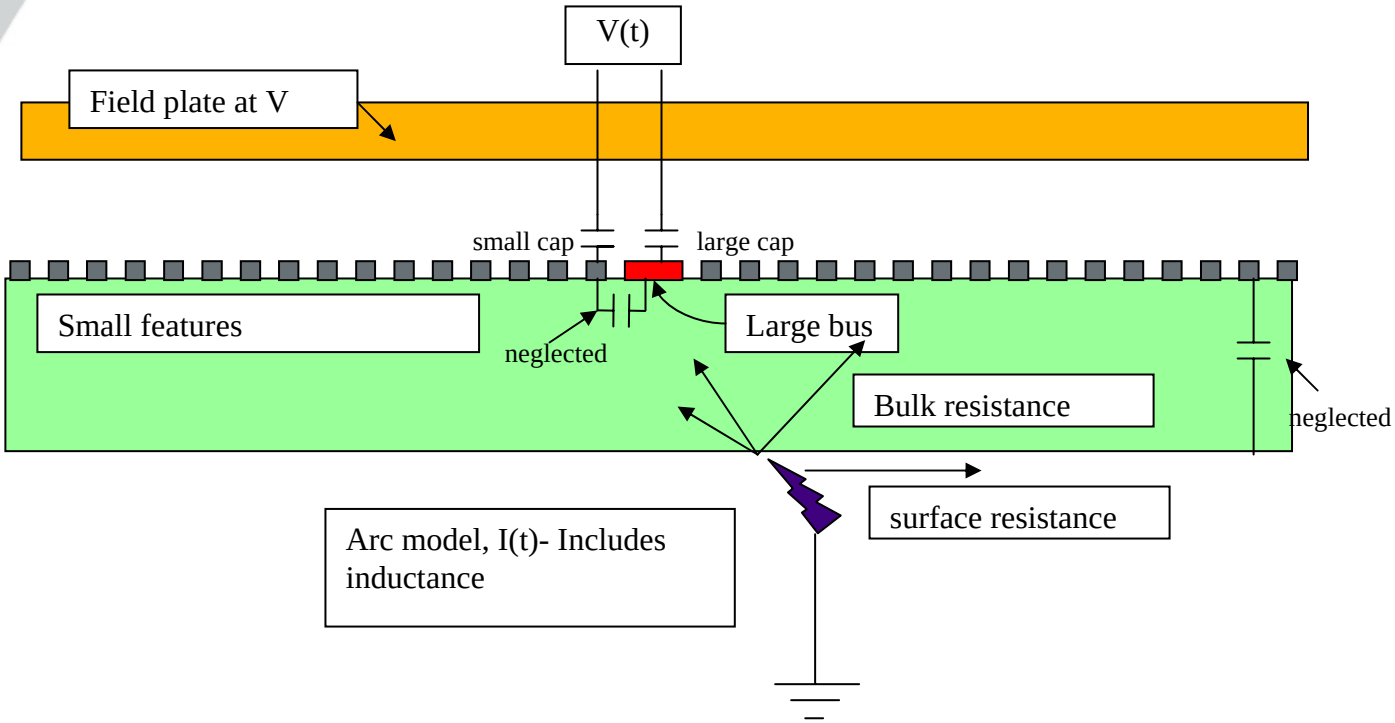
Wafer ESD Model Schematic



Modeling sequence

- Field plate (simulating charged source near wafer) is charged to the desired stressing voltage
  - This causes the entire wafer to rise or fall to the desired stressing potential
- A simulated grounded probe is then placed into electrical contact (through an arc) with the backside of the wafer to simulate a typical wafer handling electrostatic event
- The metal islands (capacitors) on the front side then discharge through the underlying silicon substrate
- The quasi-steady-state static potential and the electric field are then computed as functions of position and time while the simulation proceeds
- Voltage potentials develop between the metal islands with the highest potentials typically between neighboring islands with different capacitances

Failure Mechanism

- A fast transient leads to voltage potential between features
- Sufficiently high voltage for sufficient duration initiates Fowler-Nordheim (F-N) tunneling*
- Failure occurs when cumulative charge trapping exceeds a certain level defined as Q_{bd}

*See S. Sze, Physics of Semiconductor Devices, Second Edition, p497.

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Failure Model

- For 5 kV ESD event, peak ΔV is 50-250 volts across top side chip features.
- This ΔV may appear across thin gate oxide.
- F-N tunneling current density (J) given by $J = c_1 E^2 \exp(-c_2 / E)$
- Total charge density deposited into gate oxide during FCDM event given as $\sigma_{ox} = \int J(t)dt$.
- For FCDM event, duration is brief, but J is large.
- If $\sigma_{ox} > Q_{bd,}$ gate oxide fails irreversibly.
- This could cause failure of MOSFETs internal to DUT, not necessarily in I/O regions – more difficult to detect.
- Detection of such failures depends upon vector set fault coverage. Failure would appear as a hard functional failure, not necessarily as a parametric leakage failure

Ignoring Inter-feature Capacitance

- For this model, inter-feature capacitances are paralleled by inter-feature resistance of 1/(g*mesh spacing). This resistance is about 0.8 ohm.
- Consider a 0.8 ohm resistor in parallel with an inter-feature capacitor of 0.1 pF. Compare resistor conduction current ($\Delta V/R$) & capacitor displacement current (Cdv/dt).
- For 5 kV event, peak I_{cond} = 25 A.; peak I_{dis}=0.4 A.
- Conduction current dominates capacitor displacement current. So, we've ignored inter-feature capacitance.
- Addition of inter-feature capacitance to model is always possible at client request.

Simulation Runs

- **Variables explored**
  - Large and small capacitance values
  - Bulk wafer conductivity
  - Back surface conductivity
  - Stressing voltage
  - Zap location
- **Fixed quantities**
  - Wafer thickness
  - Feature spacing
  - Arc model with fixed voltage/length

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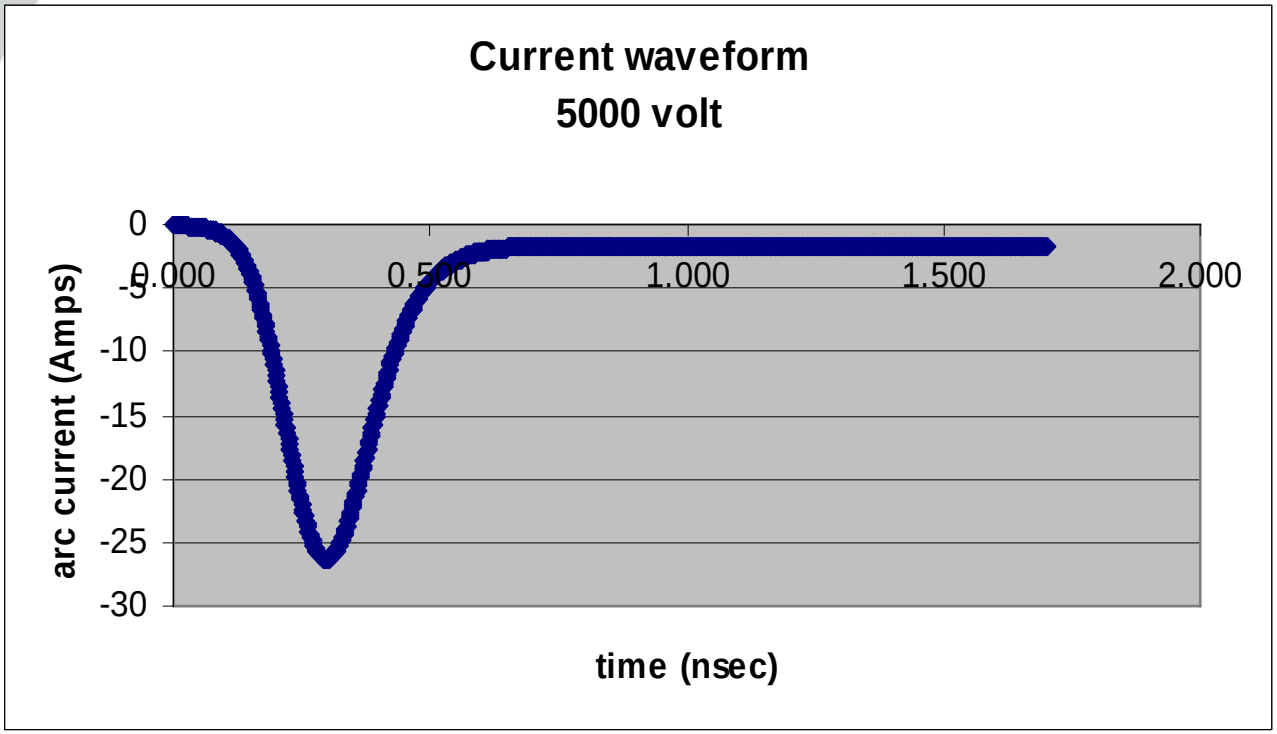
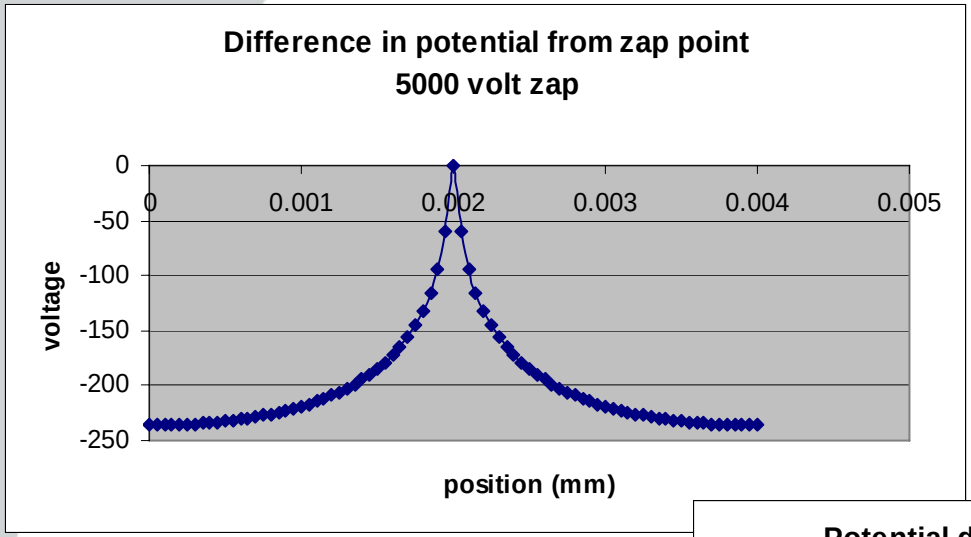
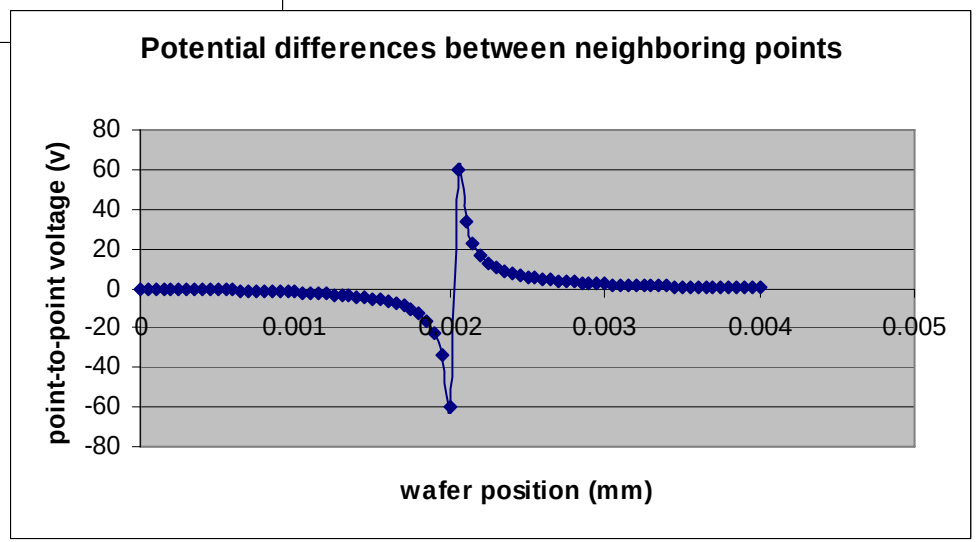
Typical waveform



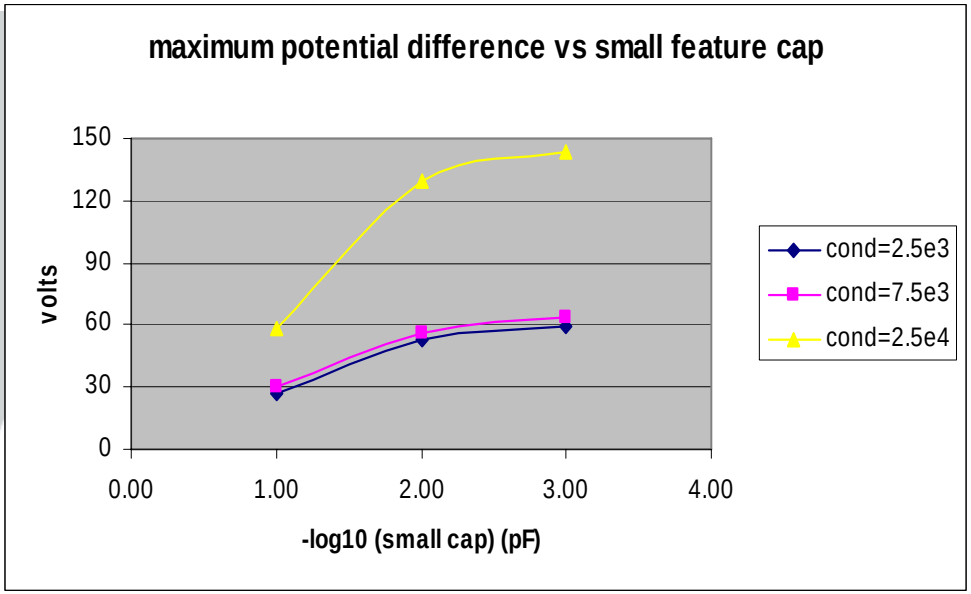
Typical wafer potential difference distributions





Software also produces animated plots of key variables

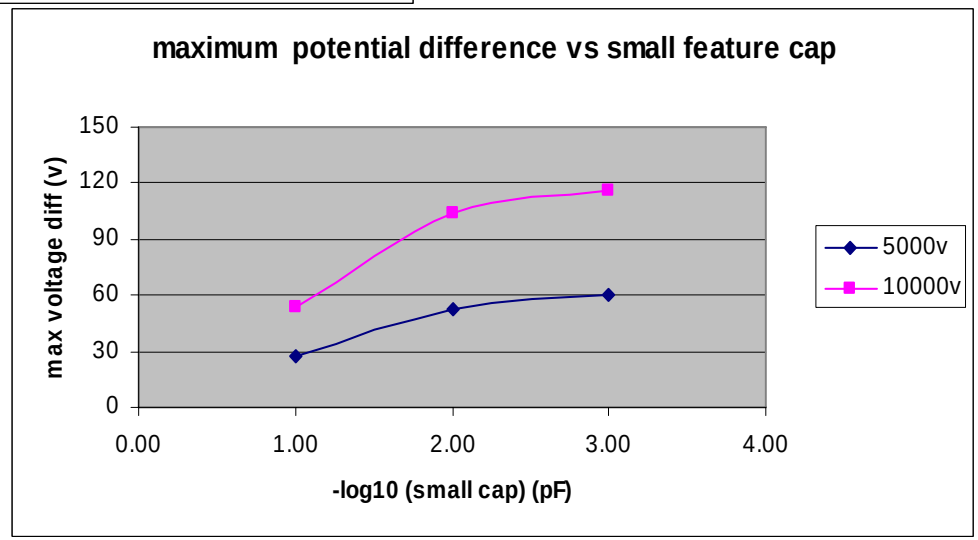
Results summary plots



Maximum potential difference vs. small feature capacitance for various conductivities and zap voltage 5kV

Maximum potential difference vs. small feature capacitance for 5kV and 10kV zaps

Bulk conductivity = 2.5e3



Summary and Conclusions

- Changes in relative capacitance with respect to charge source of neighboring features could have significant effect on voltage differentials between features on a die
- Maximum voltage potentials appear for ~100 picoseconds at or near the time of current peak and at point of larger capacitance
- Maximum feature-to-feature potentials roughly scale with zap voltage

Summary and Conclusions (cont.)

- Need to relate small-to-large capacitance range to technology evolution
- Failures would be difficult to detect based on current test techniques since they would be internal, depend on test coverage
- Status: These results suggest that relatively high voltages can be developed on wafer-like structures. Further work is required to firmly establish the "calibration" of the results using actual Q_{bd}, capacitances and conductivities