Background Statement for SEMI Draft Document 5275
REAPPROVAL OF SEMI G79-0200, SPECIFICATION FOR OVERALL DIGITAL TIMING ACCURACY

Note: This background statement is not part of the balloted item. It is provided solely to assist the recipient in reaching an informed decision based on the rationale of the activity that preceded the creation of this document.

Note: Recipients of this document are invited to submit, with their comments, notification of any relevant patented technology or copyrighted items of which they are aware and to provide supporting documentation. In this context, “patented technology” is defined as technology for which a patent has issued or has been applied for. In the latter case, only publicly available information on the contents of the patent application is to be provided.

Background
SEMI G79-0200 is long overdue for Five Year Review. This process is required by the SEMI Regulations to ensure that this standard is still valid.

At the North America (NA) Standards meetings at SEMICON West 2011, the NA Automated Test Equipment (ATE) Committee approved the letter ballot distribution for the Reapproval of SEMI G79 because it was believed that this standard is still being used by a number of companies.

Review and Adjudication Information

<table>
<thead>
<tr>
<th>Task Force Review</th>
<th>Committee Review &amp; Adjudication</th>
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<tbody>
<tr>
<td>Group: [] Ballot results to be reviewed at the NA ATE committee meeting.</td>
<td>North America Automated Test Equipment Committee</td>
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<tr>
<td>Date: →</td>
<td>Wednesday, October 26, 2011</td>
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<tr>
<td>Time &amp; Timezone: →</td>
<td>4:30 PM to 6:00 PM, Pacific Time</td>
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<tr>
<td>Location: →</td>
<td>SEMI Headquarters 3081 Zanker Road</td>
</tr>
<tr>
<td>City, State/Country: →</td>
<td>San Jose, California / U.S.A.</td>
</tr>
<tr>
<td>Leader(s): →</td>
<td>Ajay Khoche (Consultant)</td>
</tr>
<tr>
<td>Standards Staff: Paul Trio (SEMI NA) 408.943.7041 <a href="mailto:ptrio@semi.org">ptrio@semi.org</a></td>
<td>Paul Trio (SEMI NA) 408.943.7041 <a href="mailto:ptrio@semi.org">ptrio@semi.org</a></td>
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This meeting’s details are subject to change, and additional review sessions may be scheduled if necessary. Contact SEMI Standards staff for confirmation.

Telephone and web information will be distributed to interested parties as the meeting date approaches. If you will not be able to attend these meetings in person but would like to participate by telephone/web, please contact Standards staff.

If you need a copy of the document in order to cast a vote, please contact the following person within SEMI.
Paul Trio
SEMI Standards, North America
Tel: 1.408.943.7041
Email: ptrio@semi.org
SEMI Draft Document 5275
REAPPROVAL OF SEMI G79-0200, SPECIFICATION FOR OVERALL DIGITAL TIMING ACCURACY

NOTICE: This ballot contains only the following sections of the standard being proposed for Reapproval: Purpose, Scope, Limitations, Referenced Standards, and Terminology. If you would like a copy of SEMI G79 in order to vote on it, please request a copy by email from Paul Trio at ptrio@semi.org.

1 Purpose
1.1 This standard is intended to provide a minimum common definition of timing accuracy specifications for automatic semiconductor test equipment (ATE).

2 Scope
2.1 The scope of this standard includes all semiconductor ATE capable of digital functional testing. This standard does not include the following:
   - test fixturing errors,  
   - device insertion errors, and  
   - ATE performance or capability beyond timing accuracy.
2.2 This standard’s overall timing accuracy (OTA) definition serves to simplify automatic test equipment comparisons and reduce specification ambiguity.
2.3 This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory limitations prior to use.

3 Limitations
3.1 Parameters associated with the following items are not covered by the Overall Digital Timing Accuracy Specification:
   - minimum driver pulse width,  
   - comparator bandwidth,  
   - I/O round trip delay,  
   - test fixturing errors,  
   - device insertion errors,  
   - time measurement unit accuracy, and  
   - ATE capability or performance beyond timing accuracy.

4 Referenced Standards
None.

5 Terminology
5.1 Abbreviations and Acronyms
5.1.1 ATE — automatic test equipment
5.1.2 DUT — device under test
5.1.3 NR — Non-return signal format

5.1.4 RTx — return to zero, one or complement signal format.

5.1.5 SBx — surround by zero, one or complement signal format.

5.1.6 Z — driver off (high impedance)

5.2 Definitions

5.2.1 device insertion errors — error influenced by device-input capacitance and/or terminations.

5.2.2 edge — time delay created by an ATE delay generation resource.

5.2.3 performance board — printed circuit board used to interface the tester channels to the device under test.

5.2.4 pin — tester channel

5.2.5 reference load A — 500 ohms in parallel with 2.5pf (± 0.5pf) to ground

5.2.6 reference load B — 50 ohms to ground

5.2.7 reference load C —

- 50 ohms to low (for driver z to high and high to z transitions).
- 50 ohms to high (for driver z to low and low to z transitions).

5.2.8 strobe compare — monitor DUT output at a single time point.

5.2.9 test cycle — inverse of test pattern execution frequency.

5.2.10 test fixturing errors — error influenced by mismatched signal path lengths, impedance discontinuities, lumped capacitance/inductance elements, and high frequency loss due to skin effect or interconnects.

5.2.11 window compare — monitor DUT continuously during a time interval.

NOTE 1: The term “input” as it appears in this document refers to the device under test.

NOTICE: SEMI makes no warranties or representations as to the suitability of the standard(s) set forth herein for any particular application. The determination of the suitability of the standard(s) is solely the responsibility of the user. Users are cautioned to refer to manufacturer’s instructions, product labels, product data sheets, and other relevant literature respecting any materials or equipment mentioned herein. These standards are subject to change without notice.

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