NEW STANDARD: SPECIFICATION FOR DEVELOPMENTAL 450 mm DIAMETER POLISHED SINGLE CRYSTAL SILICON WAFERS

Note: This background statement is not part of the balloted item. It is provided solely to assist the recipient in reaching an informed decision based on the rationale of the activity that preceded the creation of this document.

Note: Recipients of this document are invited to submit, with their comments, notification of any relevant patented technology or copyrighted items of which they are aware and to provide supporting documentation. In this context, “patented technology” is defined as technology for which a patent has issued or has been applied for. In the latter case, only publicly available information on the contents of the patent application is to be provided.

Attached document specifies 450 mm diameter polished single crystal wafers intended for use in research and development of process and metrology equipment and fabrication processes required to manufacture high-density integrated circuits on 450 mm diameter single crystal silicon wafers. It can also be used to establish the techniques and metrology necessary to support a dimensional specification for 450 mm diameter circuit-quality (prime) wafers.

This document should be superseded by dimensional specification and technology-specific guidelines for circuit-quality wafers.

The detailed specifications for 450 mm wafers are organized in three categories to assist manufacturers in choosing the most cost effective wafers for a given application:

- Particle monitors, intended for use in evaluating the particle contamination added by a process tool.
- Lithography monitors, for development of lithographic and patterning equipment and processes. Other monitors, suitable for use in process and inspection equipment development (other than particle counting or lithography development).

The developmental wafers dimensional requirement are identical to the 450 mm mechanical handling wafers, published in SEMI M74, except wafer diameter tolerance, tightened to +/- 0.1 mm, to better reflect wafer handling and some process equipment needs.

When specifying the wafer edge profile the customers have the choice to select between two options a parameter based profile or a template based edge profile design.

Another new option available for 450 mm is a “notch-free” wafer. In addition to the regular wafers with an orientation notch, the 450 mm wafers specification allows interested customers to choose a “notch free” wafer, where the notch is replaced by a backside inscribed fiducial mark.

The results of this document be reviewed at the Int’l 450 mm Wafer TF and will be adjudicated by the European Silicon Wafer committee during their meetings at SEMICON Europa in October 7, 2009 in Dresden, Germany. Please check www.semi.org/standards for the latest meeting schedule.
NEW STANDARD: SPECIFICATION FOR DEVELOPMENTAL 450 mm DIAMETER POLISHED SINGLE CRYSTAL SILICON WAFERS

1 Purpose

1.1 The developmental wafers covered by this specification are intended for use in research and development of process and metrology equipment and fabrication processes required for manufacturing high-density integrated circuits on 450 mm diameter single crystal silicon wafers. They can also be used to establish the techniques and metrology necessary to support a dimensional specification for 450 mm diameter circuit-quality (prime) wafers.

2 Scope

2.1 This specification covers dimensional and crystallographic orientation requirements for 450 mm diameter, polished single crystal silicon wafers needed in development. This document should be superseded by dimensional specification and technology-specific guidelines for circuit-quality wafers.

2.2 A complete purchase specification requires that additional physical properties be specified along with test methods for determining their magnitude. If a test instrument is not available, the acceptance criteria should be agreed upon between supplier and customer.

2.3 This specification also contain guidance to assist equipment manufacturers and others to specify wafers for use in developing selected process equipment and unit processes.

2.4 The specification for 450 mm diameter mechanical handling wafers used in development of 450 mm semiconductor equipment such as 450 mm wafers carriers, load ports, AMHS, and robotics has already been published as SEMI M74.

2.5 This specification is not intended to be a product wafer specification.

2.6 For referee purposes, SI (System International, commonly called metric) units shall be used.

NOTICE: This standard does not purport to address safety issues, if any, associated with its use. It is the responsibility of the users of this standard to establish appropriate safety and health practices and determine the applicability of regulatory or other limitations prior to use.

3 Referenced Standards and Documents

3.1 SEMI Standards

SEMI M1 — Specifications for Polished Single Crystal Silicon Wafers

SEMI M13 — Specification for Alphanumeric Marking of Silicon Wafers

SEMI M33 — Test Method for the Determination of Residual Surface Contamination on Silicon Wafers by Means of Total Reflection X-Ray Fluorescence Spectroscopy (TXRF)

SEMI M43 — Guide for Reporting Wafer Nanotopography.


SEMI M52 — Guide for Specifying Scanning Surface Inspection Systems for Silicon Wafers for the 130 nm, 90 nm, 65 nm, and 45 nm Technology Generations

SEMI M53 — Practice for Calibrating Scanning Surface Inspection Systems Using Certified Depositions of Monodisperse Reference Spheres on Unpatterned Semiconductor Wafer Surfaces

SEMI M58 — Test Method for Evaluating DMA-Based Particle Deposition Systems and Processes

SEMI M59 — Terminology for Silicon Technology.
SEMI M67 — Practice for Determining Wafer Near-Edge Geometry from a Measured Thickness Data Array Using the ESFQR, ESFQD and ESBIR Metrics
SEMI M68 — Practice for Determining Wafer Near-Edge Geometry from a Measured Height Data Array Using a Curvature Metric, ZDD
SEMI M70 — Practice for Determining Wafer-Near-Edge Geometry Using Partial Wafer Site Flatness
SEMI M73 — Test method for extracting relevant characteristics from measured wafers edge profiles
SEMI M74 — Specifications for 450 mm Diameter Mechanical Handling Polished Wafers
SEMI MF26 — Test Methods for Determining the Orientation of a Semiconductive Single Crystal
SEMI MF42 — Test Methods for Conductivity Type of Extrinsic Semiconducting Materials
SEMI MF81 — Test Method for Measuring Radial Resistivity Variation on Silicon Wafers.
SEMI MF23 — Practice for Unaided Visual Inspection of Polished Silicon Wafer Surfaces.
SEMI MF33 — Test Method for Thickness and Thickness Variation of Silicon Wafers.
SEMI MF34 — Test Method for Bow of Silicon Wafers
SEMI MF657 — Test Method for Measuring Warp and Total Thickness Variation on Silicon Wafers by Noncontact Scanning
SEMI MF673 — Test Methods for Measuring Resistivity of Semiconductor Wafers or Sheet Resistance of Semiconductor Films with a Noncontact Eddy-Current Gage
SEMI MF951 — Test Method for Determination of Radial Interstitial Oxygen Variation in Silicon Wafers
SEMI MF1049 — Practice for Shallow Pit Detection on Silicon Wafers
SEMI MF1152 — Test Method for Dimensions of Notches on Silicon Wafers
SEMI MF1188 — Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption With Short Baseline
SEMI MF1389 — Test Method for Photoluminescence Analysis of Single Crystal Silicon for III-V Impurities
SEMI MF1390 — Test Method for Measuring Warp on Silicon Wafers by Automated Noncontact Scanning
SEMI MF1451 — Test Method for Measuring Sori on Silicon Wafers by Automated Noncontact Scanning
SEMI MF1530 — Test Method for Measuring Flatness, Thickness, and Thickness Variation on Silicon Wafers by Automated Noncontact Scanning
SEMI MF1617 — Test Method for Measuring Surface Sodium, Aluminum, and Potassium on Silicon and Epi Substrates by Secondary Ion Mass Spectrometry
SEMI MF1619 — Test Method for Measurement of Interstitial Oxygen Content of Silicon Wafers by Infrared Absorption Spectroscopy with p-Polarized Radiation Incident at the Brewster Angle
SEMI MF1621 — Practice for Determining Positional Accuracy Capabilities of a Scanning Surface Inspection System
SEMI MF1727 — Practice for Detection of Oxidation Induced Defects in Polished Silicon Wafers
SEMI MF1809 — Guide for Selection and Use for Etching Solutions to Delineate Structural Defects in Silicon
SEMI MF1810 — Test Method for Counting Preferentially Etched or Decorated Surface Defects in Silicon Wafers.
SEMI MF2074 — Guide for Measuring Diameter of Silicon and Other Semiconductor Wafers
4 Terminology

4.1 Terms and acronyms associated with silicon wafers and silicon technology are listed and defined in SEMI M59.

5 Wafer Ordering Information

5.1 Purchase orders for silicon wafers furnished to this specification shall include the following items. Values for these items are given in Tables 1

5.1.1 Crystal Growth Method (see ¶ 6.3).
5.1.2 Conductivity Type and Dopant.
5.1.3 Resistivity or Resistivity Range.
5.1.4 Lot Acceptance Procedures (see § 7).
5.1.5 Test methods for specified attributes (see § 8).
5.1.6 Certification (if required) (see § 9).
5.1.7 Packing and Package Labeling (see § 10).

5.2 Optional Criteria — The following items may also be specified in addition to those listed above if they are considered to be necessary for the application for which the wafers are to be employed (see Table 1).

5.2.1 Particulate contamination (localized light scatterer) requirements (see ¶ 6.5.2).
5.2.2 Surface defect requirements, including surface metal contamination (see ¶ 6.5.3).
5.2.3 Flatness — As specified in Appendix 1 of SEMI M1.
5.2.4 Optional wafer identification mark symbol or symbols (see ¶ 6.5.1.1).

5.3 Additional Criteria — Any additional criteria considered to be necessary for the application for which the wafers are to be employed may also be specified, as agreed between supplier and customer (see Table 1).

6 Requirements

6.1 Table 1 contains detailed specifications for 450 mm diameter wafers intended for use in development. The requirements are organize by wafer categories to assist manufacturers in choosing the most cost effective wafers for a given application.

6.2 Wafer Categories

6.2.1 Particle monitors — Wafers intended for use in evaluating the particulate contamination added by a process tool must have controlled front and back surface defect properties. Consequently, specifications are provided for front surface localized light scatterers (LLSs), edge chips, and scratches on both surfaces. If desired, a specification for back surface LLSs can be negotiated between supplier and purchaser.

6.2.2 Lithography monitors — For development of lithographic and patterning equipment and processes, both surface flatness and surface defects must be carefully controlled.

6.2.3 Other monitors — This column repeats the basic requirements for developmental wafers. Wafers in this category are not intended for use in particle counting or lithography and patterning. These wafers are suitable for use in process and inspection equipment development. When used for furnace and thermal processes development wafer back side, edge surface finish and oxygen content are critical issues in connection with the introduction of slip during high temperature processing. Bulk iron, oxidation induced stacking faults, and bulk microdefects all can influence wafer performance in thermal processing and should be controlled for critical tests; appropriate specification levels should be negotiated between supplier and purchaser.
Table 1 Specification for Developmental 450 mm Diameter Polished Single Crystal Silicon Wafers

<table>
<thead>
<tr>
<th>Item</th>
<th>Polished Wafer Type</th>
<th>SEMI Measurement Method</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Particle Monitors</td>
<td>Lithography Monitors</td>
<td>Other Monitors</td>
</tr>
<tr>
<td>1. General Characteristics</td>
<td>Cz or MCz</td>
<td>(100)</td>
<td>p or n</td>
</tr>
<tr>
<td>1.1 Growth Method</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.2 Crystal Orientation</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.3 Conductivity Type</td>
<td>p</td>
<td>p or n</td>
<td>M1, MF42</td>
</tr>
<tr>
<td>1.4 Dopant</td>
<td>B</td>
<td>B or P</td>
<td>M1, MF389</td>
</tr>
<tr>
<td>1.5 Nominal FQA radius</td>
<td>223 mm</td>
<td></td>
<td>Center referenced</td>
</tr>
<tr>
<td>1.6 Wafer surface orientation</td>
<td>+/- 1º</td>
<td></td>
<td>MF26 (x-ray)</td>
</tr>
</tbody>
</table>

2. Electrical Characteristics

<table>
<thead>
<tr>
<th>2.1 Resistivity</th>
<th>Measured @ Center Point</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1.1 p type wafers</td>
<td>0.005 - 100 ohm-cm</td>
</tr>
<tr>
<td>2.1.2 n type wafers</td>
<td>2 - 5 ohm-cm</td>
</tr>
<tr>
<td>2.2 Radial Resistivity Variation (RRG)</td>
<td>&lt;10%</td>
</tr>
</tbody>
</table>

3. Chemical Characteristics

| 3.1 Oxygen Concentration | Customer Specified | M1, MF1188, MF1366 |
| 3.2 Radial Oxygen Variation | ≤10% | MF951 |

4. Structural Characteristics

| 4.1 Dislocation Etch Pit Density | ≤10/cm² | M1, MF1809 |
| 4.2 Slip | None | M1, MF1809 |
| 4.3 Lineage | None | M1, MF1809 |
| 4.4 Twin Boundary | None | M1, MF1809 |
| 4.5 Swirl | None | M1, MF1809 |
| 4.6 Shallow pits | None | M1, MF1727 |

5. Wafer Preparation Characteristics

| 5.1 Wafer ID Marking | SEMI T7 | T7, M13 |
| 5.2 Edge surface conditions | Polished |
| 5.3 Back surface condition | Polished |

6. Dimensional Characteristics

| 6.1 Diameter | 450 +/- 0.1 mm | M1, MF2074 |
| 6.2 Notch dimensions | Depth 1.00±0.25 -0.00 mm | Angle 90 ° ± 5 ° -1 ° |
| 6.3 Orientation of Notch axis | <110> +/-1 |
| 6.4 Edge profile | M73 | An alternative, template based edge |
### Polished Wafer Type

<table>
<thead>
<tr>
<th>Item</th>
<th>Particle Monitors</th>
<th>Lithography Monitors</th>
<th>Other Monitors</th>
<th>SEMI Measurement Method</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.4.1 Front edge width</td>
<td>350 +/- 50 μm</td>
<td></td>
<td></td>
<td></td>
<td>profile is depicted in Appendix 2</td>
</tr>
<tr>
<td>6.4.2 Front bevel angle</td>
<td>22.5&quot; +/- 3&quot;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6.4.3 Front shoulder radius</td>
<td>202.5 +/- 42.5 μm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6.4.4 Back shoulder radius</td>
<td>202.5 +/- 42.5 μm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6.4.5 Back bevel angle</td>
<td>22.5&quot; +/- 3&quot;</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6.4.6 Back edge width</td>
<td>350 +/- 50 μm</td>
<td></td>
<td></td>
<td>MF333</td>
<td>Measured @ Center Point</td>
</tr>
<tr>
<td>6.5 Wafer Thickness</td>
<td>925 +/- 25 μm</td>
<td></td>
<td></td>
<td>MF533</td>
<td></td>
</tr>
<tr>
<td>6.6 GBIR, less than</td>
<td>10 μm</td>
<td>3 μm</td>
<td>10 μm</td>
<td>MF1530</td>
<td></td>
</tr>
<tr>
<td>6.7 Bow, max</td>
<td>Customer Specified</td>
<td></td>
<td></td>
<td>MF334</td>
<td></td>
</tr>
<tr>
<td>6.8 Warp, max</td>
<td>100 μm</td>
<td>50 μm</td>
<td>100 μm</td>
<td>MF1390</td>
<td></td>
</tr>
<tr>
<td>6.9 Flatness/SFQR</td>
<td>42 nm</td>
<td></td>
<td></td>
<td>MF1530</td>
<td></td>
</tr>
<tr>
<td>6.10 Nanotopography</td>
<td>Customer specified</td>
<td></td>
<td></td>
<td>M43</td>
<td></td>
</tr>
<tr>
<td>6.11 ERO</td>
<td>Customer specified</td>
<td></td>
<td></td>
<td>M67, M68, M70</td>
<td></td>
</tr>
</tbody>
</table>

### 7. Front Surface Chemistry

#### Surface Metal

<table>
<thead>
<tr>
<th></th>
<th>≤1 x 10^10 per cm^2</th>
<th>MF1617 (SIMS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sodium</td>
<td>≤1 x 10^10 per cm^2</td>
<td>MF1617 (SIMS)</td>
</tr>
<tr>
<td>Aluminum</td>
<td>≤1 x 10^10 per cm^2</td>
<td>MF1617 (SIMS)</td>
</tr>
<tr>
<td>Potassium</td>
<td>≤1 x 10^10 per cm^2</td>
<td>MF1617 (SIMS)</td>
</tr>
<tr>
<td>Chromium</td>
<td>≤1 x 10^10 per cm^2</td>
<td>MF1617 (SIMS)</td>
</tr>
<tr>
<td>Iron</td>
<td>≤1 x 10^10 per cm^2</td>
<td>MF1617 (SIMS)</td>
</tr>
<tr>
<td>Nickel</td>
<td>≤1 x 10^10 per cm^2</td>
<td>MF1617 (SIMS)</td>
</tr>
<tr>
<td>Copper</td>
<td>≤1 x 10^10 per cm^2</td>
<td>MF1617 (SIMS)</td>
</tr>
<tr>
<td>Zinc</td>
<td>≤1 x 10^10 per cm^2</td>
<td>MF1617 (SIMS)</td>
</tr>
<tr>
<td>Calcium</td>
<td>≤1 x 10^10 per cm^2</td>
<td>MF1617 (SIMS)</td>
</tr>
</tbody>
</table>

### 8. Front Surface Inspection Characteristics

<table>
<thead>
<tr>
<th></th>
<th>None</th>
<th>MF1, MF523</th>
</tr>
</thead>
<tbody>
<tr>
<td>8.1 Scratches</td>
<td>None</td>
<td>M1, MF523</td>
</tr>
<tr>
<td>8.2 Pits (COP)</td>
<td>Customer Specified</td>
<td>M1, MF523</td>
</tr>
<tr>
<td>8.3 Haze</td>
<td>Customer Specified</td>
<td>M1, MF523</td>
</tr>
<tr>
<td>8.4 Localized Light</td>
<td>0.16 per cm^2</td>
<td>0.32 per cm^2</td>
</tr>
<tr>
<td></td>
<td>M1, M52</td>
<td></td>
</tr>
</tbody>
</table>
### 6.3 Material and Manufacture

The material shall consist of wafers cut from ingots grown by either the normal Czochralski or the magnetic Czochralski method, at the supplier’s option.

### 6.4 Dimensions and Permissible Variations

Wafers shall conform to the dimensions and dimensional tolerances as specified for the attributes listed in Table 1.

**6.4.1 Shape**

Although the warp value specified in Table 1 is expected to be adequate for many developmental purposes, it is now recognized that warp, even with correction for gravitational sag, is not a suitable metric for specifying wafer shape for all applications. Processing may induce additional warp.

**6.4.2 Sori**

Sori is an attribute that may be specified as agreed between the supplier and the purchaser in lieu of warp. (see SEMI MF1451)

**6.4.3 Bow**

Values will be specified by the customer, depending on his application requirements.

**6.4.4 Flatness**

GBIR and SFQR are specified in Table 1. NT and ERO values shall meet customer requirements as specified in the purchase order.

**NOTE 1:** This is a wafer specification. Equipment specifications may have tighter requirements.

**6.4.5 Fiducial Mark**

A notch in conformance with the dimensions and tolerances of Figure 1 as described in M1 ¶ 6.6.1.

**6.4.5.1 Optional inscribed fiducial**

Without a notch, but with a fiducial mark inscribed on the wafer backside as described in Appendix 1.

**6.4.6 Back Surface Finish**

The back surface shall be polished.

**6.4.7 Edge Profile**

Parameter based profile. 450 mm edge profile consists of straight bevel, circular shoulder and straight apex like that of other diameter wafers. The specifications of the edge width, shoulder radius and the bevel angle are shown in the Table 1. The edge profile shall conform to the following requirements at all points on the wafer periphery (except interior portions of notches which are to be finished in accordance with the provisions of the purchase order or contract).

**6.4.7.1 Optional template based profile**

As described in M1 ¶ 6.6.2 is detailed in Appendix 2.

**6.4.7.2 Edge Surface Finish**

The edge surface finish is specified to be “polished,” which is meant to imply a surface condition and not a particular processing technique.
6.4.8  *Fixed Quality Area* — The central region of the wafer with a radius of 223 mm is designated as the fixed quality area (FQA).

**NOTE 2**: In SEMI M1, the FQA is referenced to the edge of a wafer of nominal diameter by the nominal edge exclusion. For 450 mm wafers, it is necessary to standardize the method for determining the wafer center; therefore, the FQA is being center referenced. The equivalent nominal edge exclusion for the specified FQA radius is 2 mm. To obtain the maximum benefit from this specification requirement, all equipment should be center referenced rather than edge referenced.

**NOTE 3**: It should also be noted that a larger FQA radius (smaller value of nominal edge exclusion) may be required for circuit-quality 450 mm diameter wafers.
6.5 Other requirements

The wafers shall conform to the surface orientation and fiducial axis orientation requirements as specified in Table 1.

NOTE 4: The angular surface orientation tolerance specified in Table 1 is sufficient for wafers intended for general use where channeling is to be avoided in ion implantation. For applications where maximum channeling along the [100] direction perpendicular to the (100) wafer surface plane is desired, the surface orientation tolerance must be tightened as discussed in ¶ 7.1 of SEMI M1.

6.5.1 All 450 mm wafers shall be marked with a two-dimensional matrix code symbol on the back surface outside the fixed quality area as soon after slicing as practical in the manner specified in SEMI T7 in order to provide both identification of these wafers and traceability of each wafer, going back to the ingot from which it was cut. The back surface is identified as the wafer surface with the two-dimensional matrix code symbol.

6.5.1.1 Optionally the user may specify an additional back-surface mark as shown in Figure 2. This mark contains alphanumeric characters with:

- The same message characters as the SEMI T7 mark and appropriate checksum characters as defined by SEMI M13 and
- Character string as specified in SEMI M13.

6.5.2 Particulate Contamination (Localized Light Scatterer or LLS) Requirements — Particulate contamination requirements are specified in Table 1. Particle monitors wafers have tighter requirements than other monitor wafers.

6.5.3 Surface Defect Requirements including surface metal contamination levels, are specified in Table 1.

6.5.4 The wafers shall conform to such other physical characteristics listed in SEMI M1 as may be specified in the purchase order or contract.
7 Sampling

7.1 Unless otherwise specified, ASTM Practice E 122 shall be used to define the sampling plan. When so specified, appropriate sample sizes shall be selected from each lot in accordance with ANSI/ASQC Z1.4. Each quality characteristic shall be assigned an acceptable quality level (AQL) or lot tolerance percent defective (LTPD) value in accordance with ANSI/ASQC Z1.4 definitions for critical, major, and minor classifications. If desired and so specified in the contract or order, each of these classifications may alternatively be assigned cumulative AQL or LTPD values. Inspection levels shall be agreed upon between the supplier and the purchaser.

8 Test Methods

8.1 Table 1 of SEMI M1 contains a listing of SEMI, ASTM, DIN, and JEIDA/JIS and ISO test methods that may apply to the testing of specified attributes of developmental 450 mm diameter silicon wafers.

9 Certification

9.1 Upon request of the purchaser in the contract or order, manufacturer’s or supplier’s certification that the material was manufactured and tested in accordance with this specification, together with a report of the test results, shall be furnished at the time of shipment.

9.2 In the interest of controlling inspection costs, the supplier and the purchaser may agree that the material shall be certified as “capable of meeting” certain requirements. In this context, “capable of meeting” shall signify that the supplier is not required to perform the appropriate tests as included in the purchase order or contract (see § 8). However, if the purchaser performs the test and the material fails to meet the requirement, the material may be subject to rejection.

10 Packing and Package Labeling

10.1 Special packing requirements shall be subject to agreement between the supplier and the purchaser. Otherwise all wafers shall be handled, inspected, and packed in such a manner as to avoid chipping, scratches, and contamination and in accordance with the best industry practices to provide ample protection against damage during shipment.

10.2 Wafers supplied under this specification shall be identified by appropriately labeling the outside of each box or other container and each subdivision thereof in which it may reasonably be expected that the wafers will be stored prior to further processing. Wafer box labels shall include as a minimum the following information in accordance with SEMI T3:

- Customer Assigned Product Identification Number,
- Lot Number,
- Vendor Identification Code,
- Labeling Date, and
- Quantity.

10.3 The lot number shall provide access to information concerning the nominal diameter, conductivity type, dopant, orientation, resistivity range, and fabrication history of the particular wafers in that lot. Such information shall be retained on file at the manufacturer’s facility for at least one month after that particular lot has been accepted by the purchaser, or for a longer time if so specified in the purchase order or contract.
APPENDIX 1: 450 mm DEVELOPMENTAL WAFER WITH INSCRIBED FIDUCIAL MARK

NOTICE: The material in this appendix is an official part of SEMI Mxx and was approved by full letter ballot procedures on date tbd by the global Silicon Wafer Committee.

A1-1 The inscribed fiducial mark should consist of a continuous line inscribed on the back of the wafer edge on a <110> crystallographic axis as described in Table A1-1 and Figure A1-1.

Table A1-1 Inscribed Fiducial Orientation Mark Specifications

<table>
<thead>
<tr>
<th>Item</th>
<th>Specifications</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fiducial orientation mark general characteristics</td>
<td>Wafer backside</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Continuous line</td>
<td></td>
</tr>
<tr>
<td>SEMI coordinate position</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Starting</td>
<td>0.00, -222.5 +/- 0.1mm</td>
<td></td>
</tr>
<tr>
<td>Ending</td>
<td>0.00, -224.0 mm</td>
<td></td>
</tr>
<tr>
<td>Inscribed mark length</td>
<td>1.5 +/-0.1 mm</td>
<td></td>
</tr>
<tr>
<td>Laser marking:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>diameter</td>
<td>100 +/-0,- 20 µm</td>
<td>Center to center</td>
</tr>
<tr>
<td>spacing</td>
<td>125 +/-0,- 10 µm</td>
<td></td>
</tr>
<tr>
<td>depth</td>
<td>60 +/-0,- 20 µm</td>
<td></td>
</tr>
<tr>
<td>Inscribed fiducial mark orientation in relation to</td>
<td></td>
<td></td>
</tr>
<tr>
<td>crystal axis</td>
<td>&lt;110&gt; +0/-1°</td>
<td></td>
</tr>
</tbody>
</table>

Figure A1-1
Schematics of the Inscribed Orientation Fiducial Mark on the Backside of the Wafer
APPENDIX 2: 450 mm DEVELOPMENTAL WAFER EDGE PROFILE SPECIFICATION USING TEMPLATE

NOTICE: The material in this appendix is an official part of SEMI Mxx and was approved by full letter ballot procedures on date tbd by the global Silicon Wafer Committee.

NOTICE: This edge profile specification option is intended for the customers who chose to use a template based specification instead of the parameter based profile specified in Table 1. These two specifications differ, therefore it is critical that the edge profile specification method should be agreed between the customer and the supplier.

A2-1 Edge Profile using Template Specification. (see Fig A2-1)

A2-1.1 In M74, edge profile is specified by M1 T/4 template. It is extended to specify the edge profile of 450 mm developmental wafer using new tighter template considering edge width and bevel angle tolerances. Rather new type of specification table and template are used to specify the edge profile of developmental wafer for quick recognition of the edge profile that contains all specification information.

A2-2 Edge Profile Specification

A2-2.1 Edge profile of 450 mm developmental wafer consists of straight bevel, circular shoulder and straight apex like that of other diameter wafers. Center line of the template is same as specified in Table 1. Distance of outer and inner template line from the center line is specified as template width. It is shown in the Table A2-1. Edge width, bevel angle and shoulder radius within this template should meet their tolerances. The parameter base spec is totally contained into it. Any details that are not shown in Figure A2-1 or in Table A2-1 are subject for agreement between the supplier and the user.

Figure A2-1

Edge Profile Template of 450 mm Developmental Wafer

NOTE 1: Only one-half of the edge profile and template are shown. This edge profile and template are not scalable and are not intended for use in measuring wafer thickness.

NOTE 2: Edge profile should be smooth without protrusion or sharp corner.

NOTE 3: The test method for the template specified edge is detailed in M1 ¶ A3-4.2
Table A2-1 Specifications for 450 mm Diameter Developmental Wafer Edge Profile Template

<table>
<thead>
<tr>
<th>Center Line</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Edge width</td>
<td>350 µm</td>
</tr>
<tr>
<td>Bevel angle</td>
<td>22.5°</td>
</tr>
<tr>
<td>Shoulder radius</td>
<td>202.5 µm</td>
</tr>
<tr>
<td>Apex length</td>
<td>182.2 µm</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Width</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Inward and Outward</td>
<td>30 µm</td>
</tr>
</tbody>
</table>

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