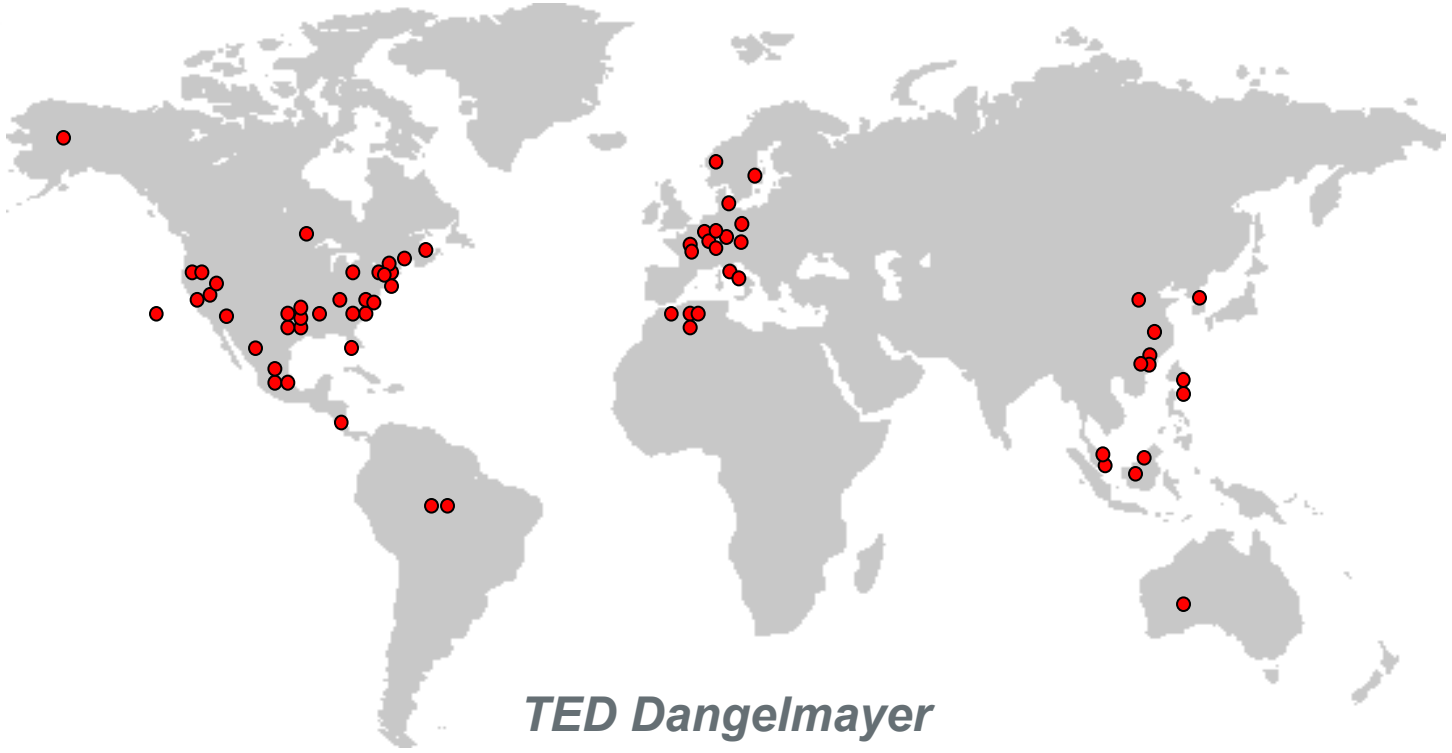
Dangelmayer ASSOCIATES, L.L.C.
Trusted ESD Programs Since 1978

Perfect ESD Storm!

CDM & Class 0 Converge in Backend



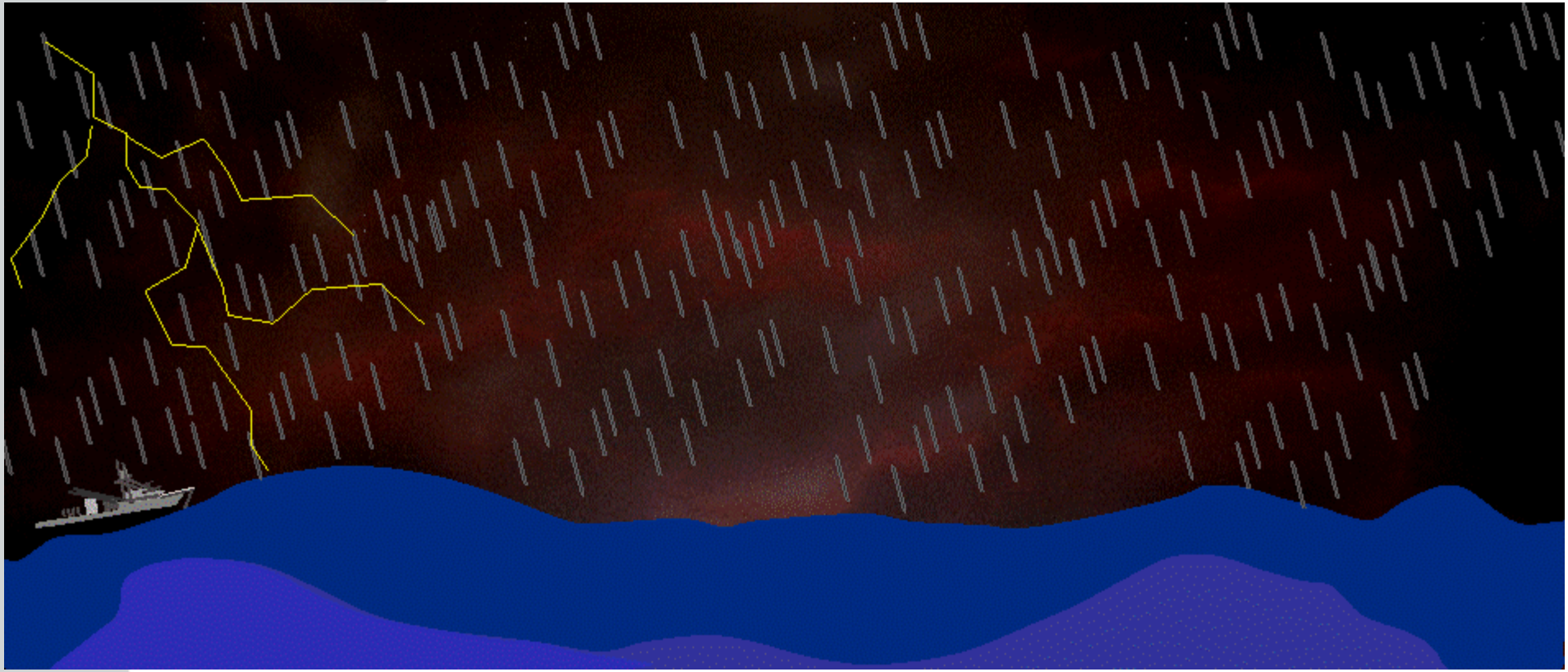
TED Dangelmayer
President & CEO
www.dangelmayer.com

Outline

- Introduction
- CDM Overview
- Lessons from the recent past
- Industry Class 0 Trend
  - It is Real This Time!
- Backend CDM Issues
- CDM & Class 0 Countermeasures
- Conclusions

CDM + Class 0 Trend =

"The Perfect ESD Storm"!



Class 0 – Rapidly Growing Trend

CDM Technology not Understood by Most Co's

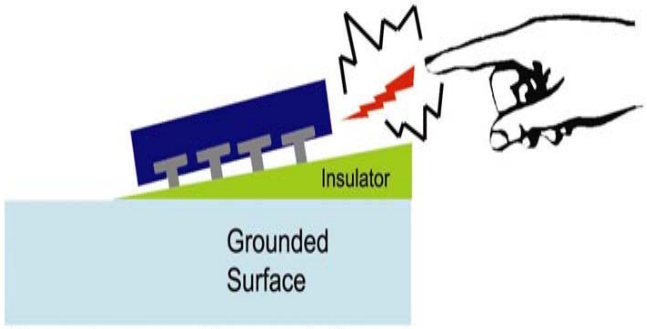
CDM = 95% of ESD Failures

CDM Overview

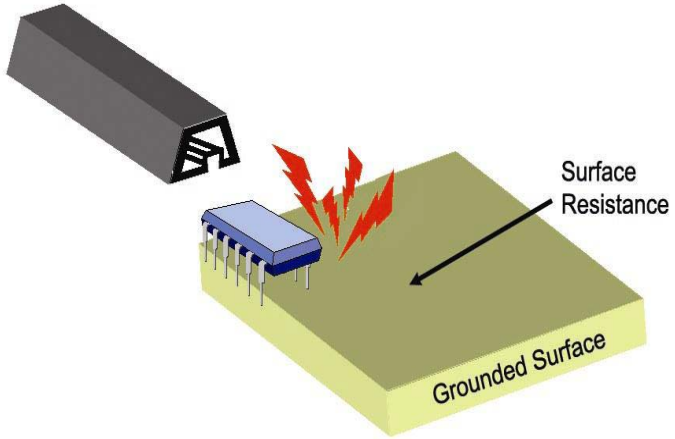
Emergence of CDM ESD

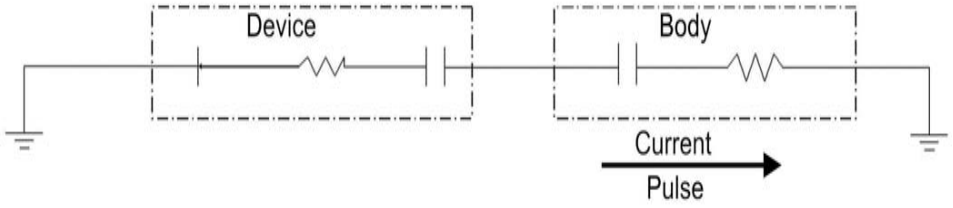
(90% to 95% of ESD Failures Today)

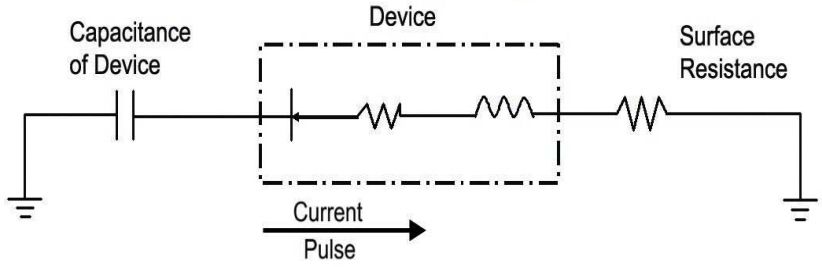
Human Body Model → **Charged Device Model**



Charged personnel (ungrounded) zapping a device placed on a grounded surface (discharge from finger to pin to chip to ground).





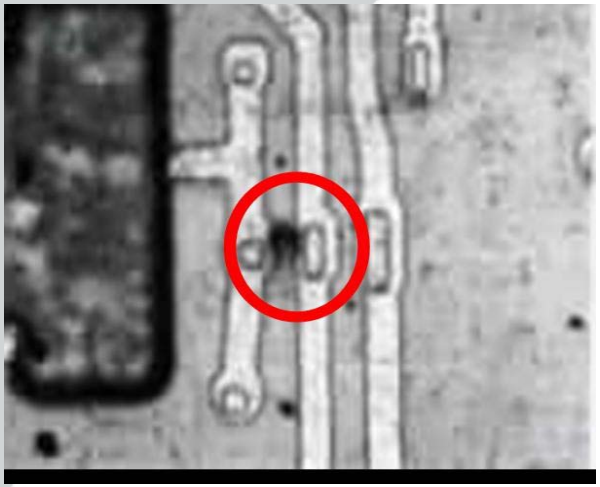


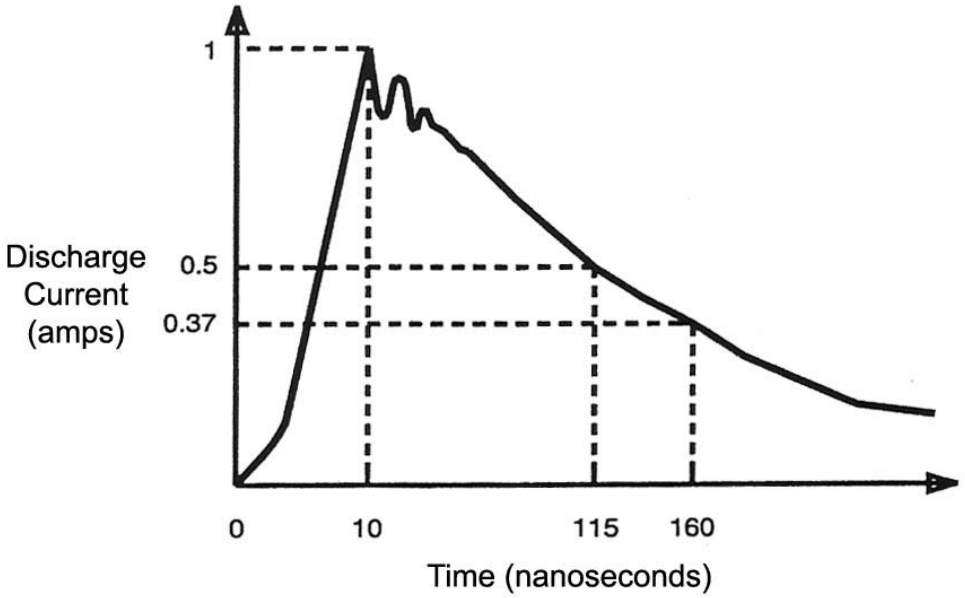
CDM Video

Tweezer Video

CDM and related metal-metal discharge events cause 95% of current ESD problems. This will continue to be the underlying driver for ESD control.

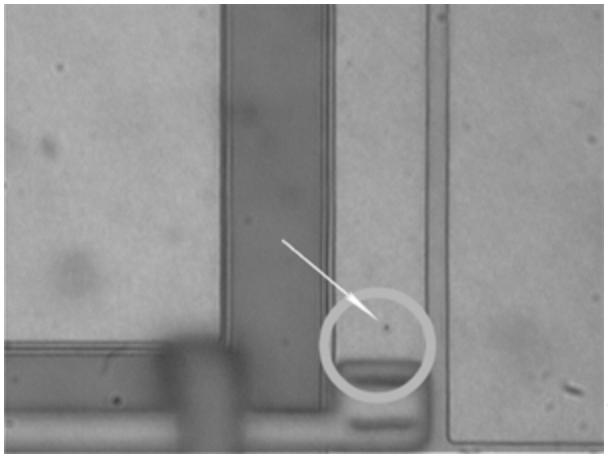
HBM

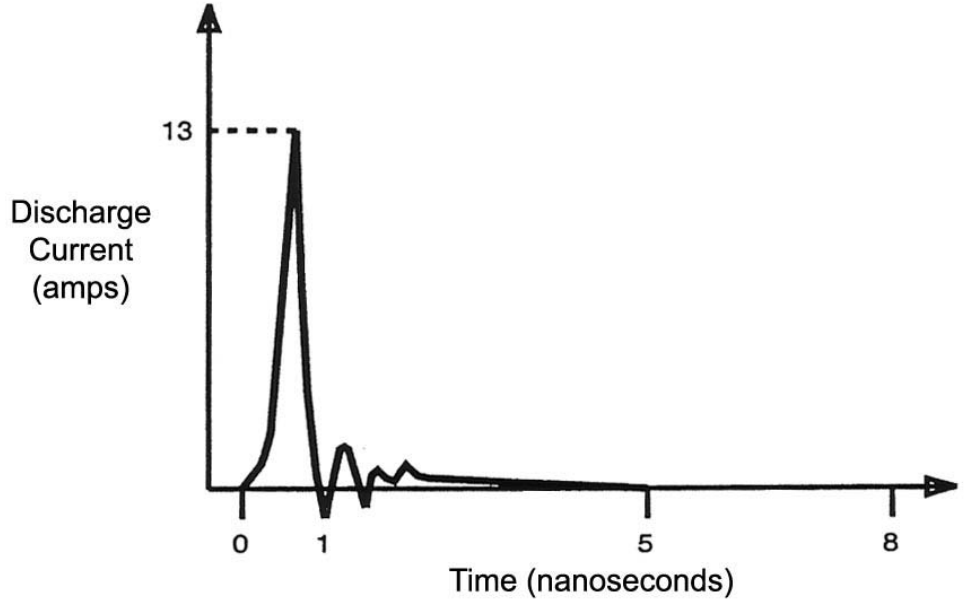




A. HBM ESD pulses

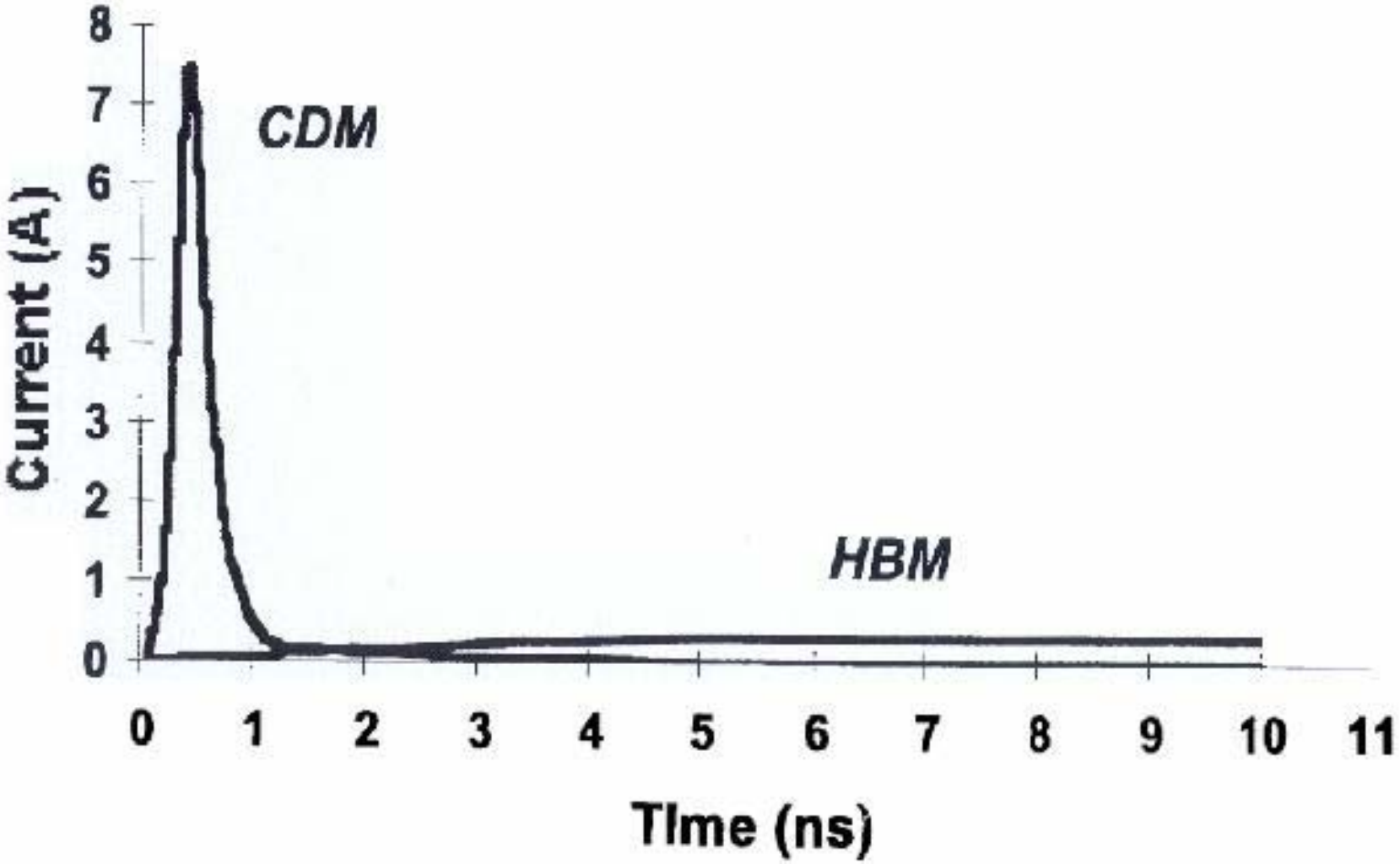
CDM





B. CDM ESD pulses

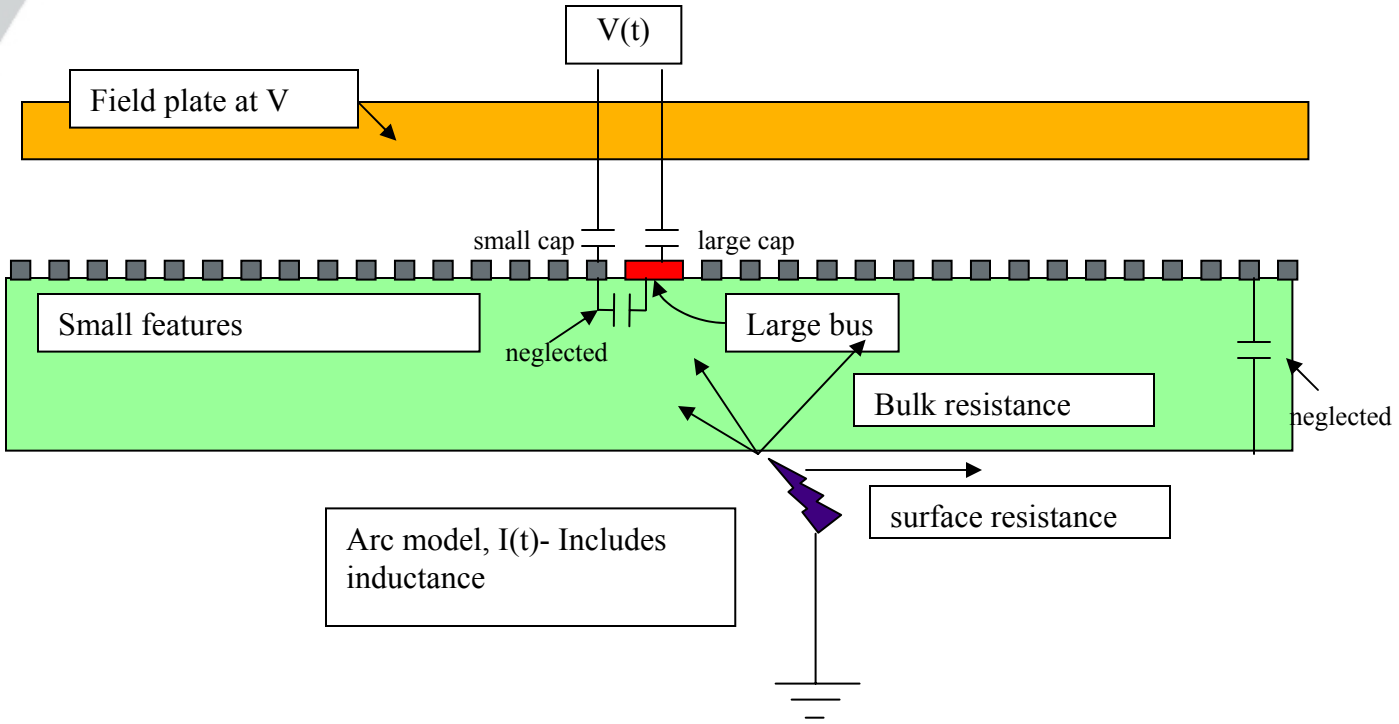
HBM and CDM Waveforms (500v)



Lessons from the Recent Past

Wafer ESD Model Schematic

Wafers Will Experience ESD Damage with Technology Trend!

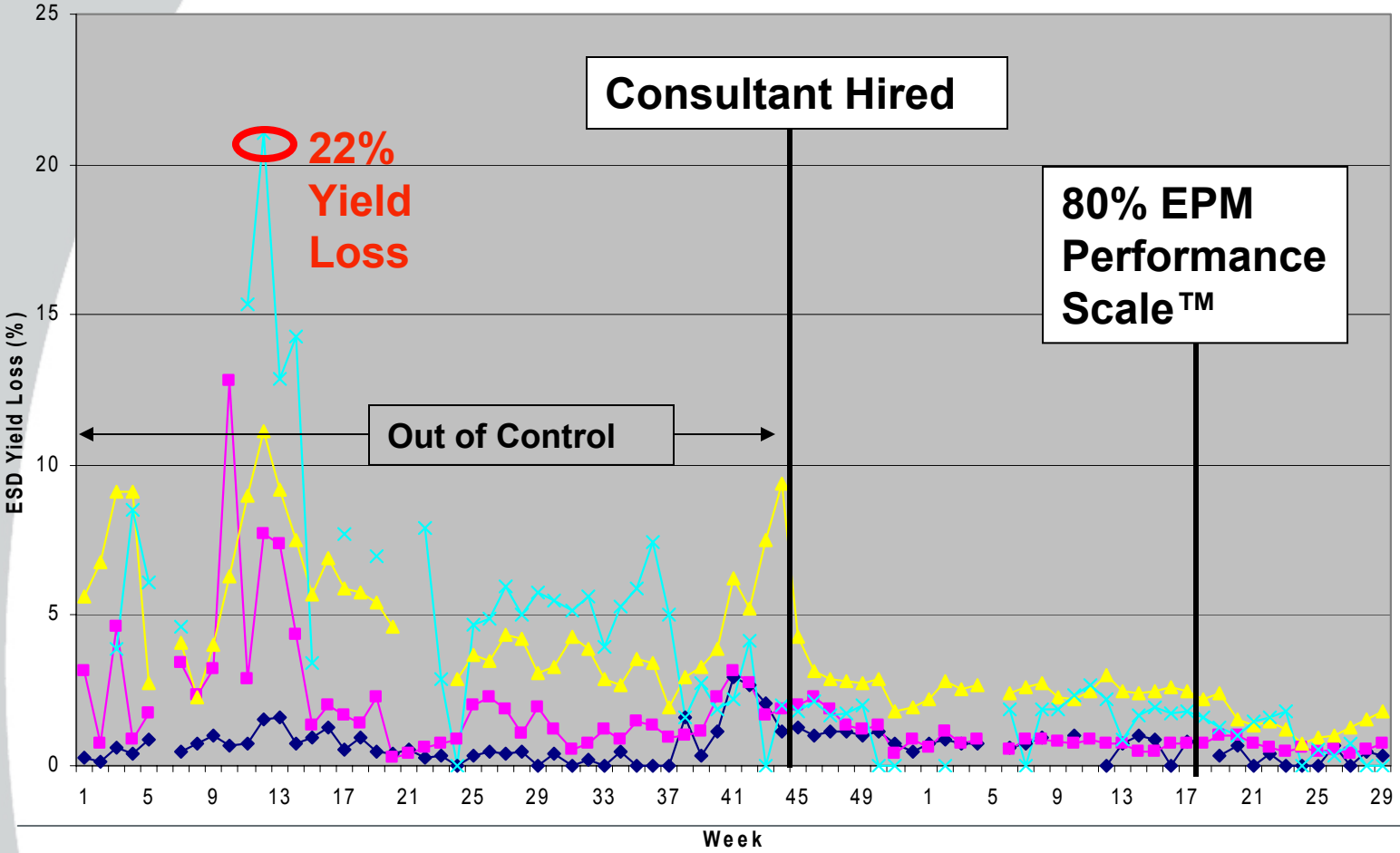


Wafer Saw Example

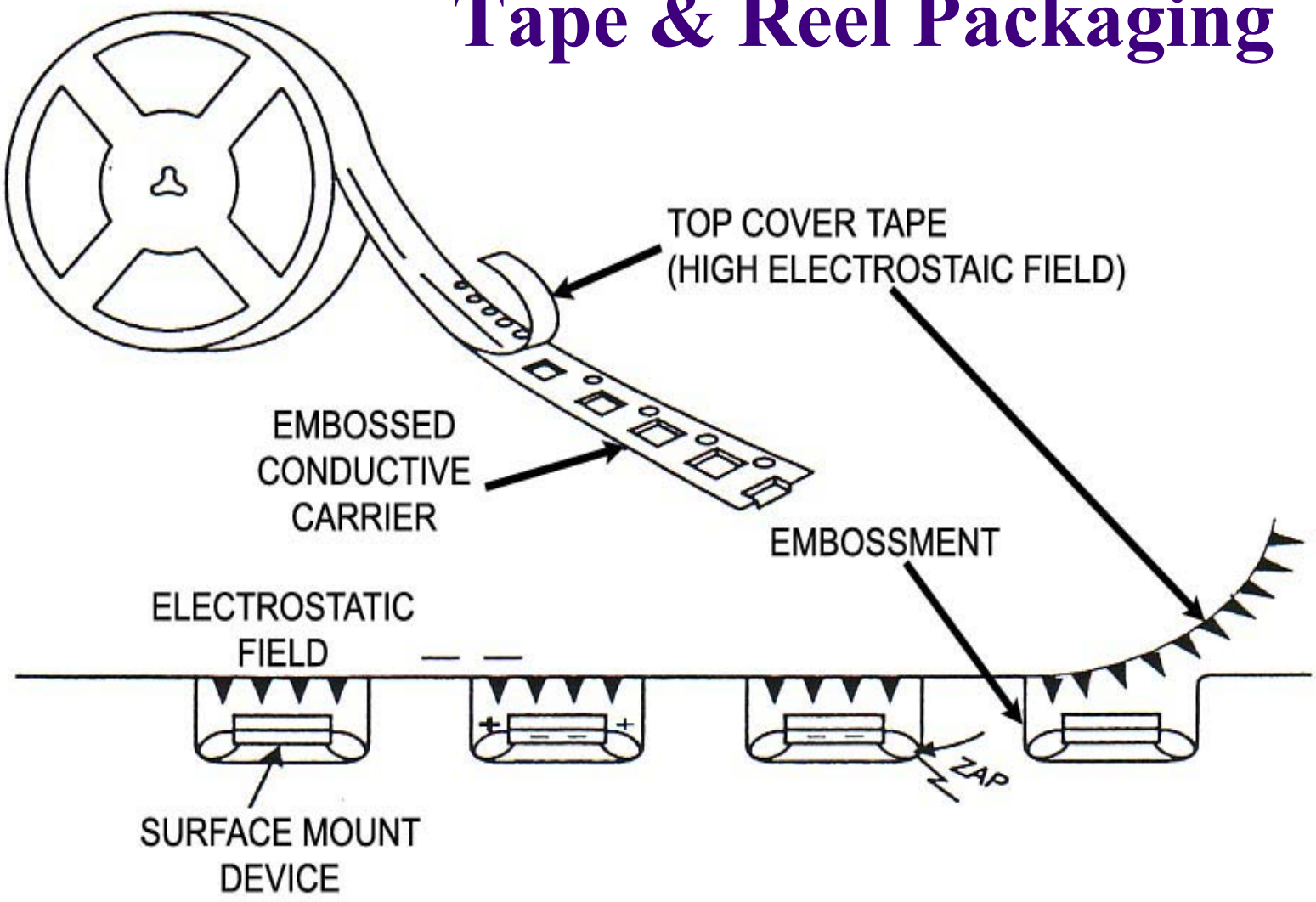
- CDM Threshold – 35 Volts
- 92.2% Defective at Wafer Saw
- Failure Analysis
  - CDM Damage

Class 0 Case Study
Corresponding Yield Improvements

Overall ESD Yield Loss Improvements



Class 0 CDM Failure Induced by Tape & Reel Packaging



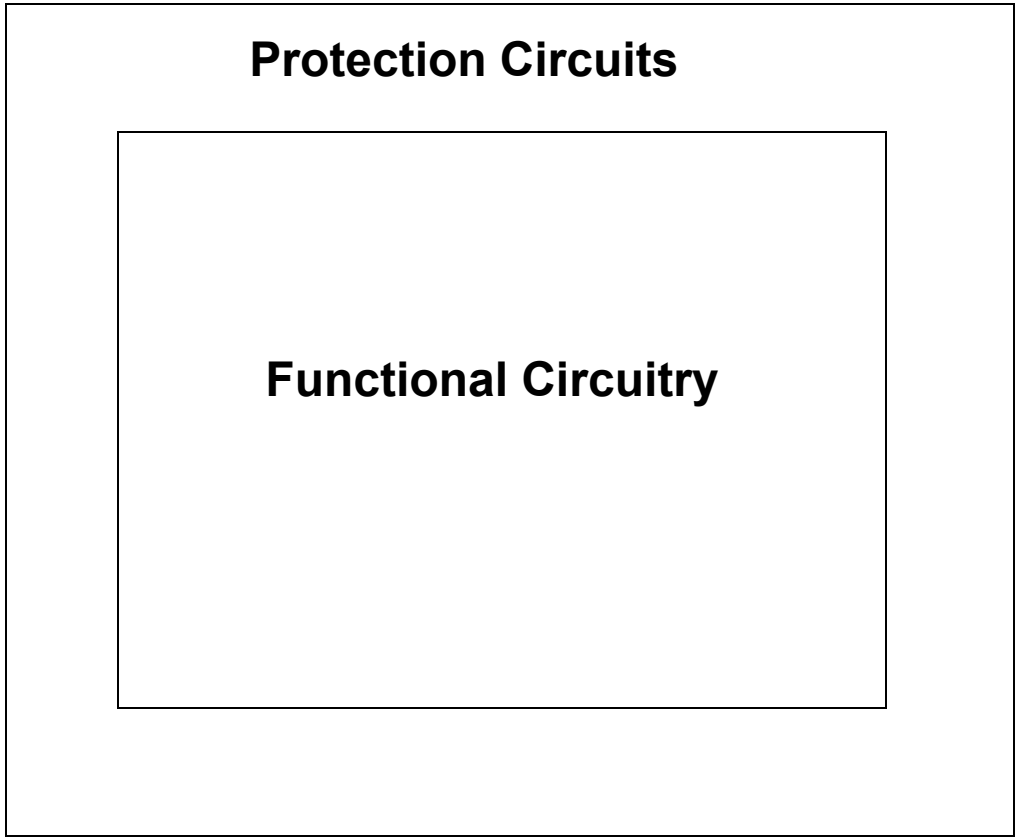
Industry Trends

It is real this time!

Typical IC With Protection Circuitry

Protection Circuits Constrained or Omitted By:

- **Technology Node Feature Sizes**
- **Circuit Functionality**
- **I/O Density**
- **Speed**



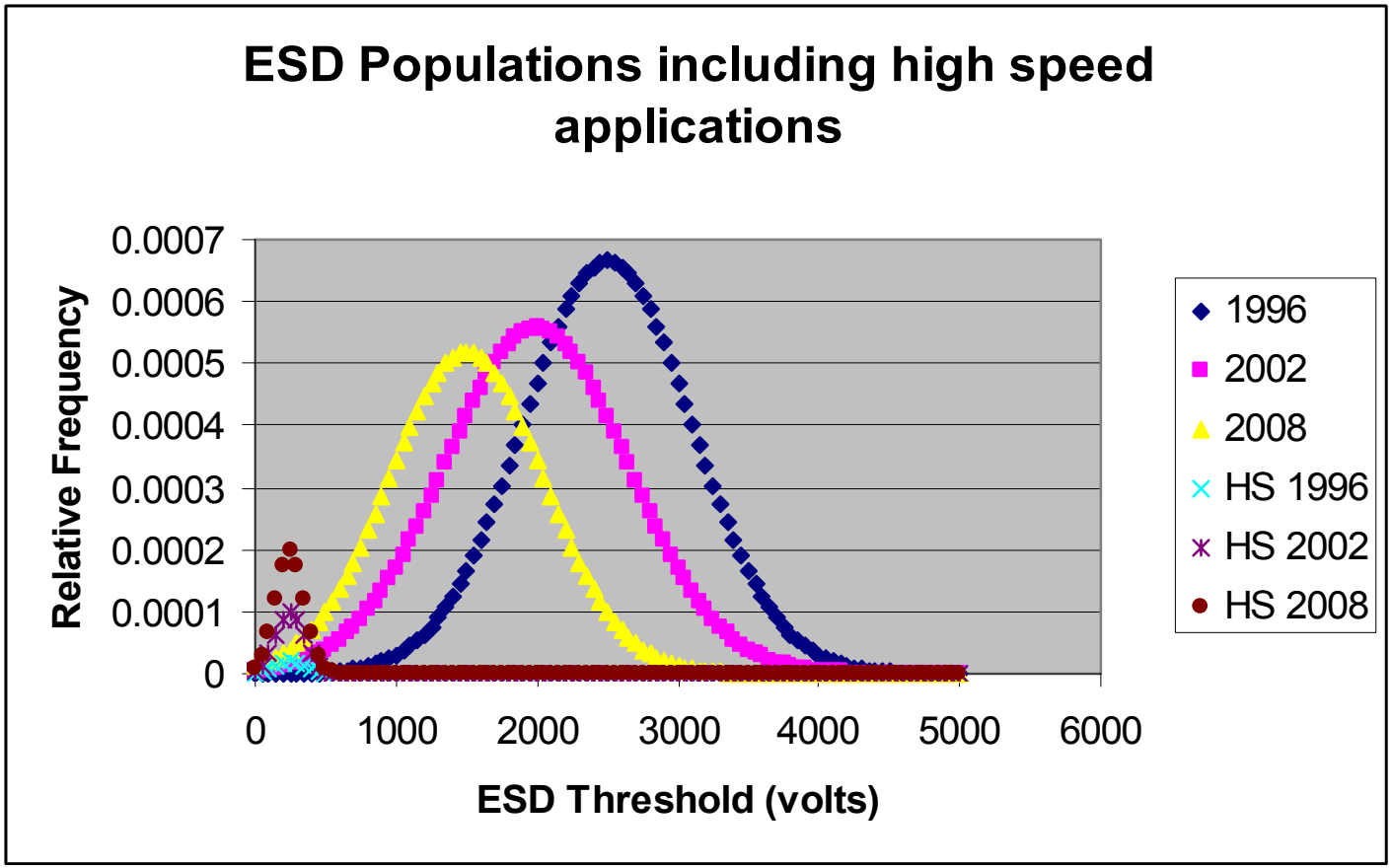
2003 ITRS

A recent SEMATECH benchmarking study of integrated circuit suppliers indicated that ESD will be one of the top three reliability concerns within the next 5 years and already is with certain products!

Year	2000	2002	2003	2004	2005	2006	2007	2008	2009	2012	2015	2018
Technology Node	180nm	130nm	100nm	90nm	80nm	70nm	65nm	55 nm	50nm	32nm	25nm	18nm
Maximum allowable electrostatic field on facility surfaces	200 V/cm	150 V/cm	125 V/cm	100 V/cm	90 V/cm	80 V/cm	70 V/cm	60 V/cm	50 V/cm	35 V/cm	25 V/cm	18 V/cm
Maximum allowable static charge on devices	2.5–10 nC (250–1000 V)	2.0 nC (200 V)	1.5 nC (150 V)	1 nC (100 V)	0.8 nC (80 V)	0.65 nC (65 V)	0.5 nC (50 V)	0.35 nC (35 V)	0.25 nC (25 V)	0.125 nC (12.5 V)	0.10 nC (10 V)	0.08 nC (8 V)
Maximum allowable electrostatic field on wafer and photomask surfaces	200 V/cm	150 V/cm	125 V/cm	100 V/cm	90 V/cm	80 V/cm	70 V/cm	60 V/cm	50 V/cm	35 V/cm	25 V/cm	18 V/cm

ESD Threshold Populations including high speed applications

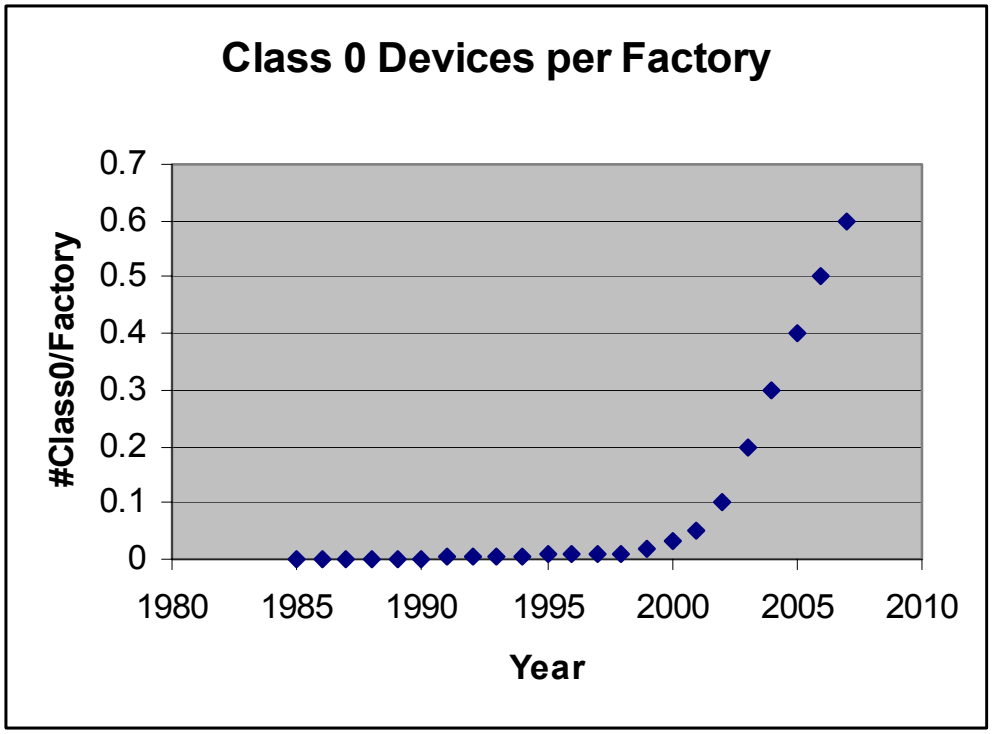
Distribution becoming bimodal



Class 0 Devices per Factory

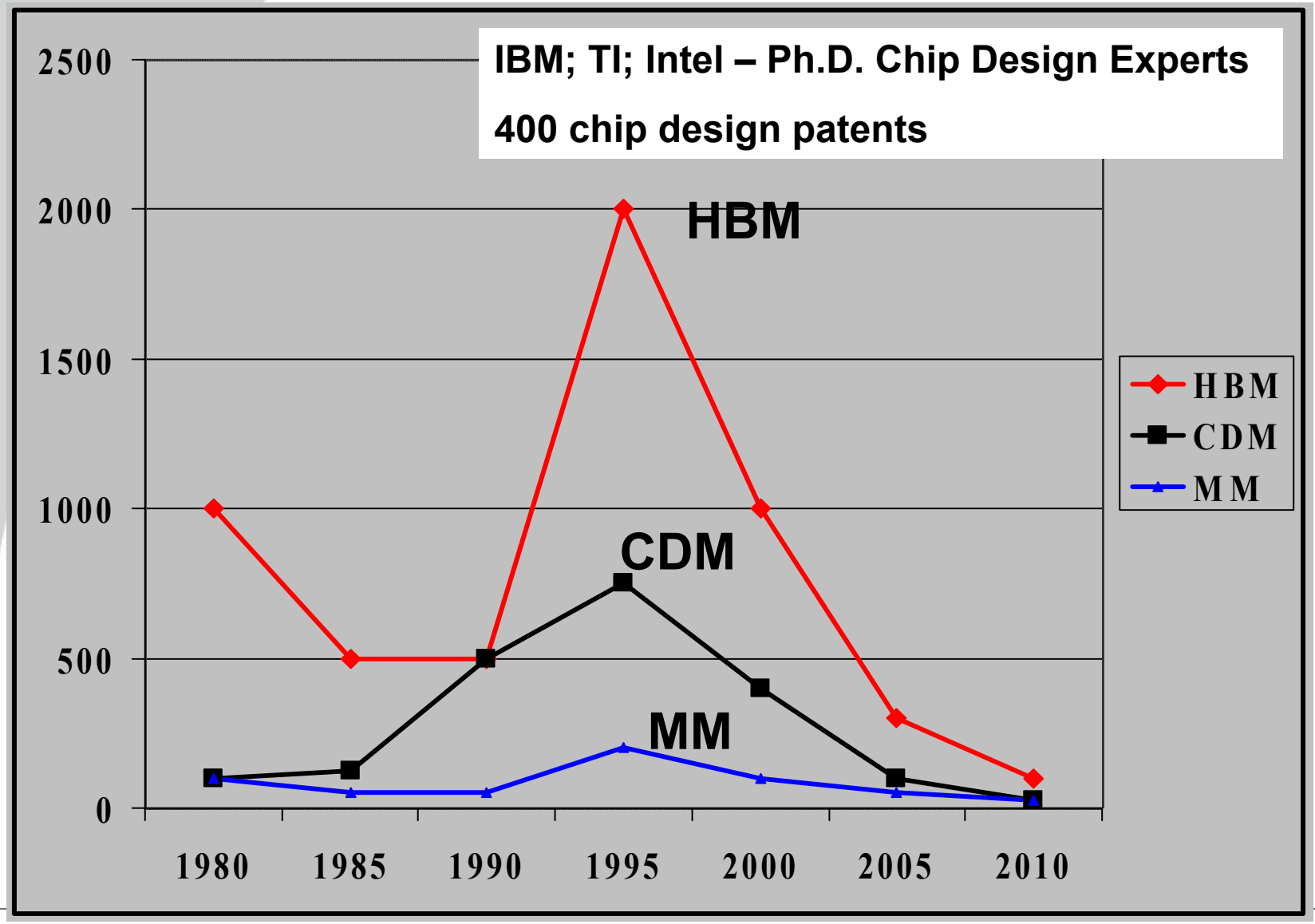
Class 0:

Virtually all Factories by 2010



ESDA Technology Roadmap

(IC Chip Design Experts: "With Our Best Effort")



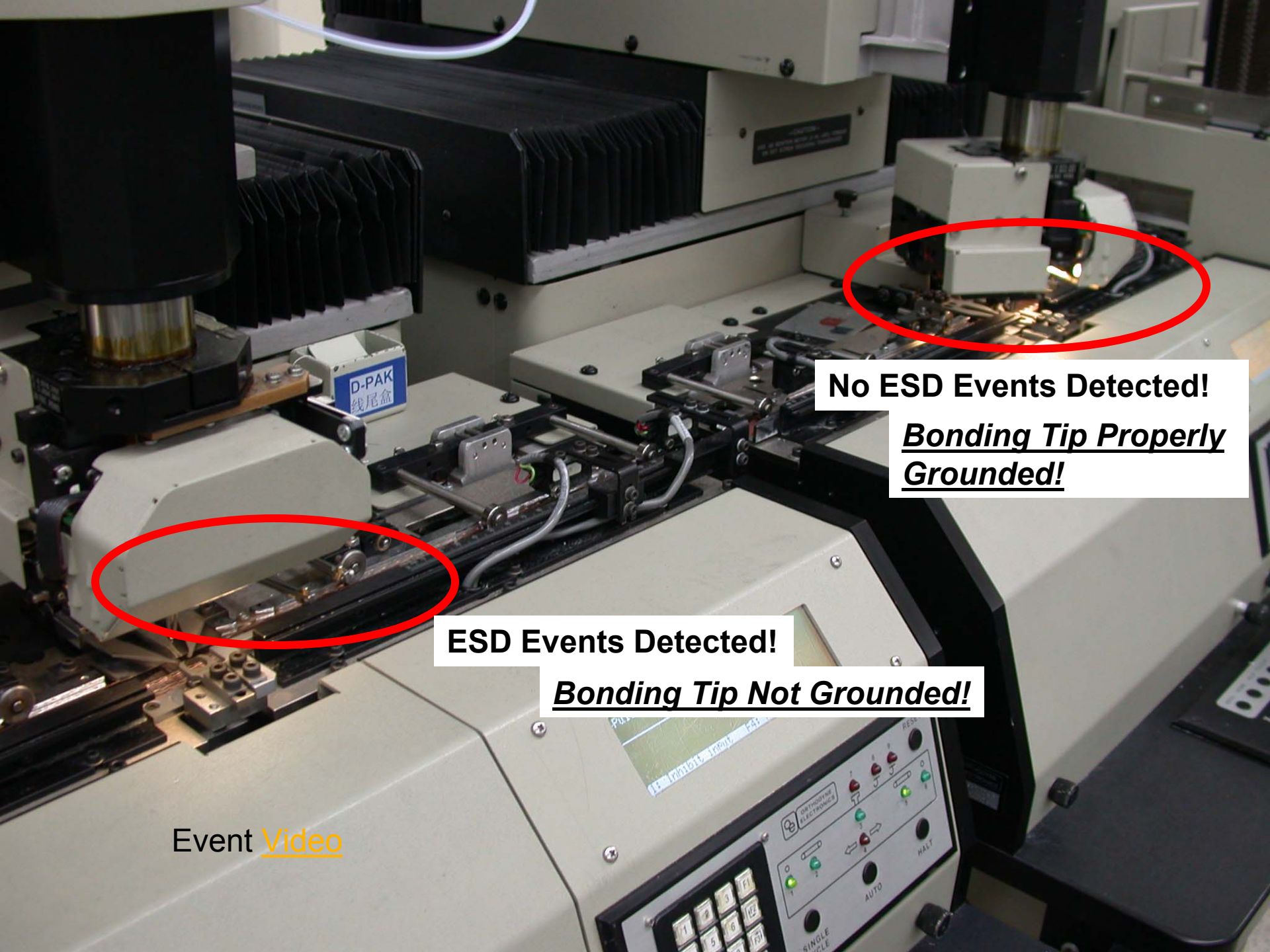
Sources of Trend Confirmation

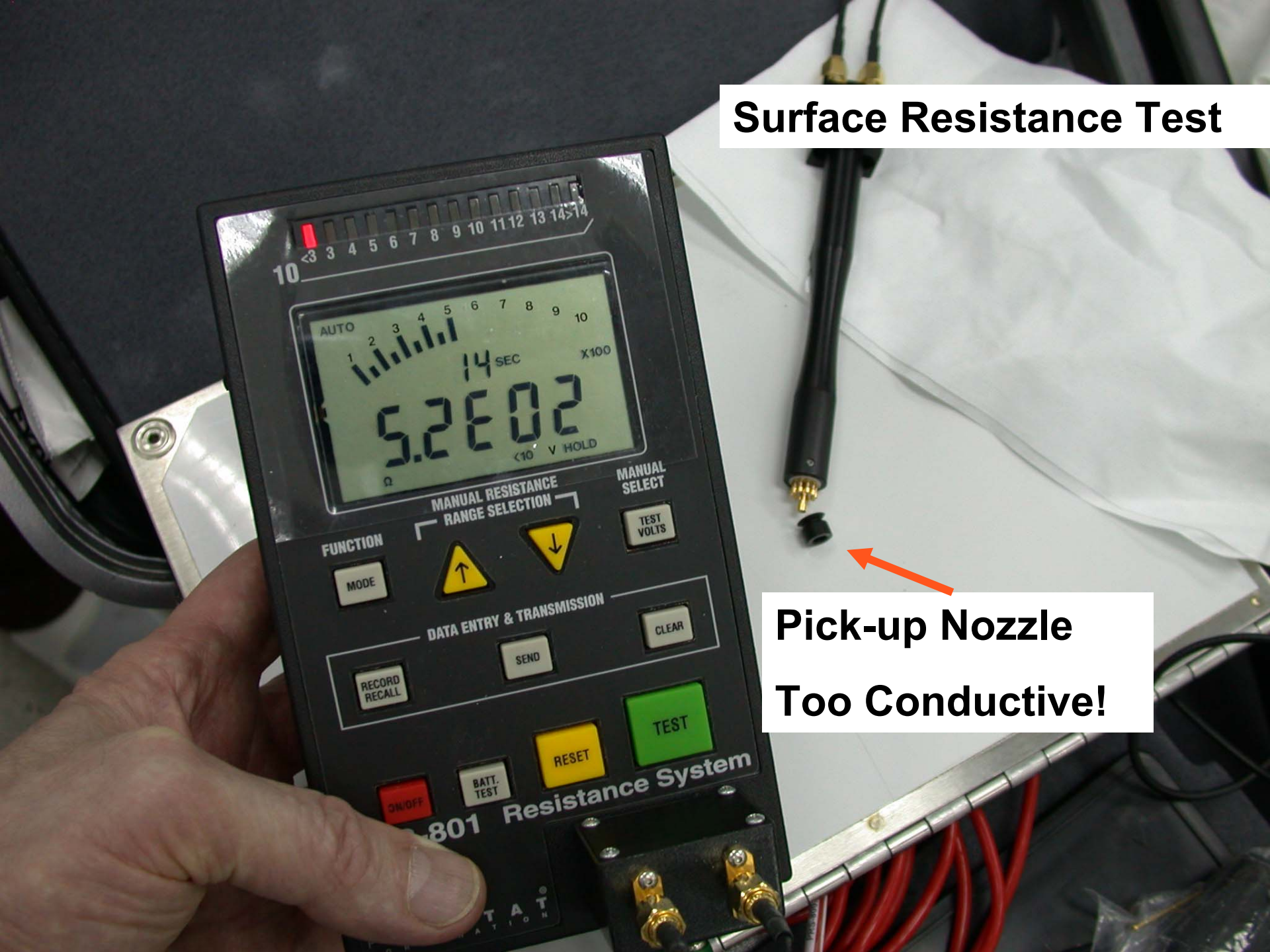
- ESD Association Roadmap
- SEMETECH – ITRI Roadmap
- DA Customer Reports / Literature Analysis
- ESD Stress Test Labs
- Stress Test Equipment Manufacturers
- IC Mfg/Design: Intel; TI; IBM; AMD etc.
  - Lowering 2000 volts HBM to 1000 volts
- FA Labs
- Subcontractors – Foxconn; Jabil; Solectron etc.
- OEM's – Cisco, Nokia, etc.

Backend CDM Issues


APR 1 2004


2.1E03
PRS-801 Resistance System
PROSTAT
TEST
1 12:44 PM


D-PAK
线尾盒
No ESD Events Detected!
Bonding Tip Properly Grounded!
ESD Events Detected!
Bonding Tip Not Grounded!
Event Video
AUTO
HALT
SINGLE CYCLE


Surface Resistance Test
Pick-up Nozzle
Too Conductive!
AUTO
14 SEC
X100
5.2E02
V HOLD
MANUAL RESISTANCE RANGE SELECTION
MANUAL SELECT
FUNCTION
MODE
TEST VOLTS
DATA ENTRY & TRANSMISSION
CLEAR
SEND
RECORD RECALL
TEST
RESET
BATT. TEST
ON/OFF
Resistance System

CDM video

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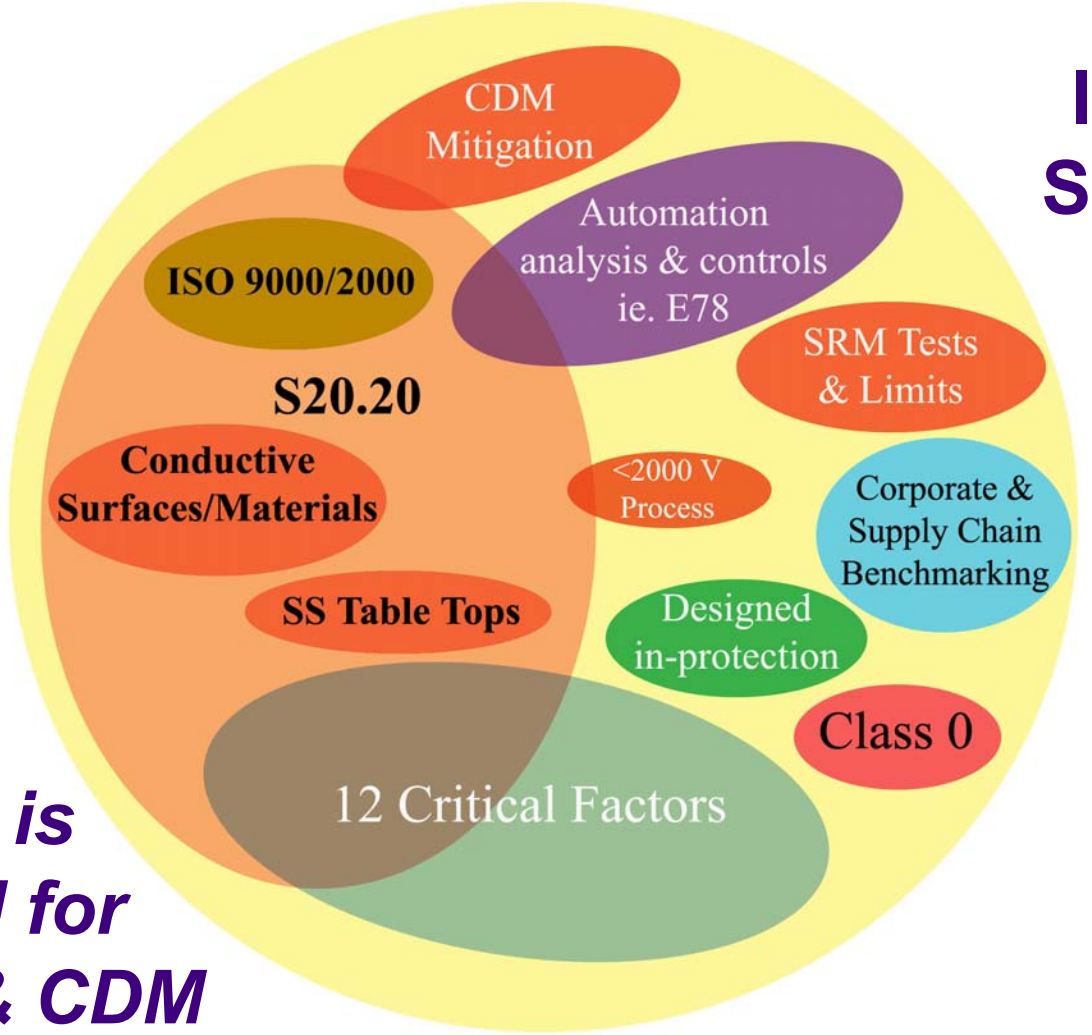
CDM & Class 0 Countermeasures

ESDA S20.20
Scope: HBM >100V

Best Industry Standard



Note:
Tailoring is Essential for Class 0 & CDM

MR Head Lessons Learned

- **Conventional ESD Methods Did Not Work!**
  - Below 100 Volts
  - Ionization Too Slow
  - Incomplete Coverage with Ionization
- **Expect a Paradigm Shift @ 100 volts**
  - Assume Device Still Charged!
- **New Control Methods**
  - Eliminate Metal-to-Metal Contact
  - Substitute “Soft Landings” with Dissipative Materials

Pogo Video

Semitron Video

Conclusions

CDM + Class 0 Trend = Perfect ESD Storm!

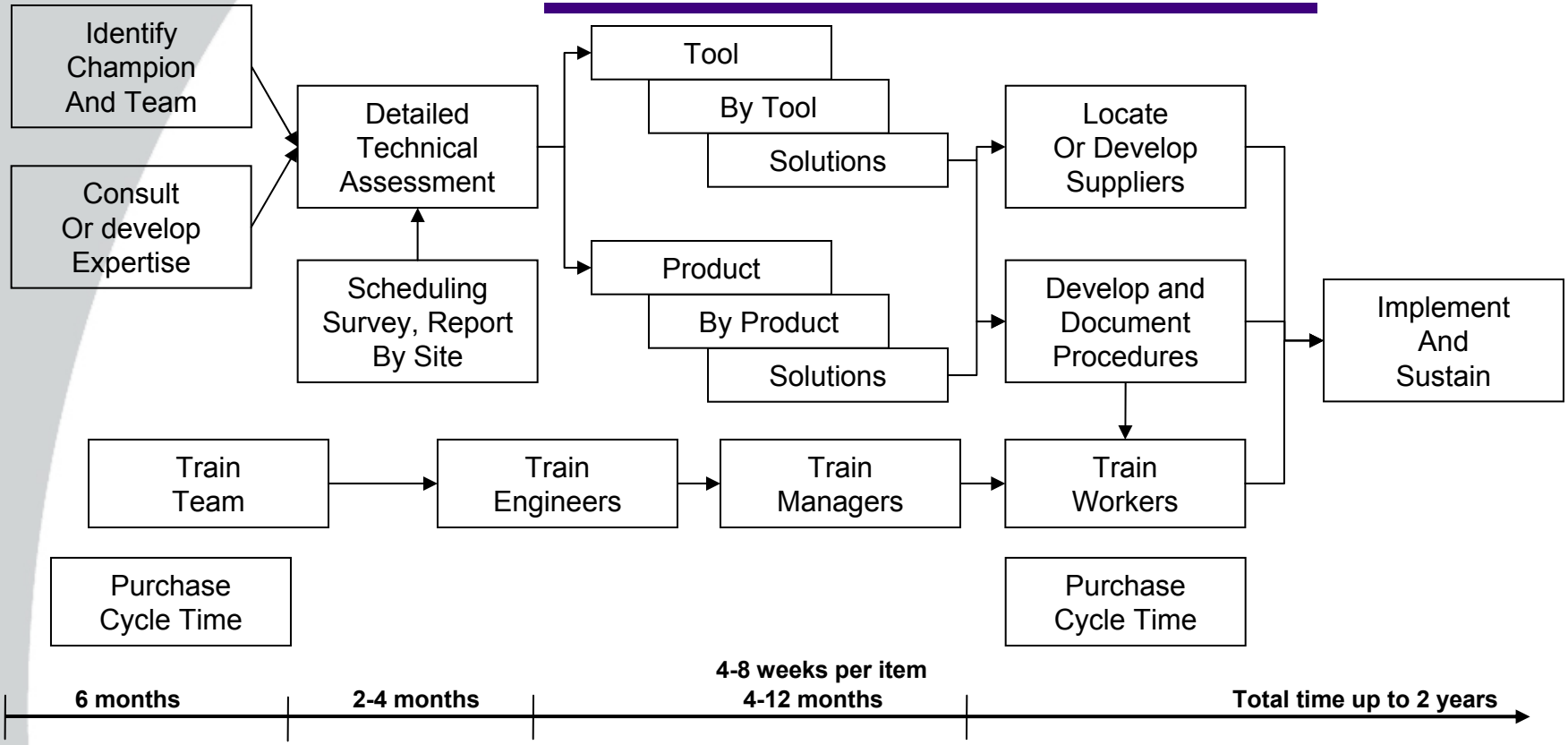
Trend Drivers:

- **Class 0:**
  - Virtually All Factories By 2010!
  - It Takes Two Year To Prepare
- **Trends Driven By**
  - Exploding Consumer Markets
  - High Volume Production
- **Designed-in Protection Circuits Limited**
  - By Speed Of Application And I/O Density

Impact On Control Procedures:

- **Standard Control Procedures**
  - Insufficient But Necessary
- **Paradigm Shift In Control Techniques**
  - Occurs At 100 Volts
  - Must Assume Product Is Still Charged
  - Ionization Often Not Sufficient
- **Metal-to-metal Contact Must Be Eliminated**
- **EMI/ESD Event Testing Is Essential**

Class 0 - Are You Ready?
It Takes 2 Years!



Initiate -> Assess -> Design -> Develop -> Implement

HS1203