STEP: E142 Substrate Mapping and Device Traceability

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STEP: E142 Substrate Mapping and Device Traceability

Program Outline

1:00 Keynote: Peter Andersen, Intel
1:15 Background and Overview
  • Introduction to the SEMI E142 the Standard – Dave Huntley, Kinesys Software (1:15)
1:30 The Industry Need
  • Implementing SEMI E142: A Case Study – Steve Chelstrom, Freescale (1:30)
  • The Scope of SEMI E142 – Andre van der Geijn, Philips (2:00)
  • EMI E142 Map and Process Examples – Dave Huntley, Kinesys Software (2:30)
3:00 Break
3:15 Traceability and Marking
  • Wafer Level Die Marking and SEMI E142 – Aidan Cunningham, GSI Lumonics (3:35)
  • Laser Marking and SEMI E142 – Josef Pfaffinger, Rofin Sinar Laser (3:55)
  • RFID Marking and E142 – Winthrop Baylies, BayTech Group (4:15)
4:35 The Future
  • Factory to Factory Integration with SEMI E142 – Dave Huntley, Kinesys Software (4:35)
4:50 Panel Discussion

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Biographies of presenters

**Winthrop A. Baylies**, founder of BayTech Group, is a specialist in international semiconductor, flat panel display, computer disk drive and general gauging technologies. He graduated from Harvard with a BA in Physical Sciences. His career includes over 20 years of management in the Electronics industry. A former chairman of ASTM F1 Committee on Electronics, Win received the ASTM Award of Merit and was elected an Honorary Fellow of the Society. He is a technical architect on the North American FPD Committee, Co-chair of the N.A. Traceability Committee, and was instrumental in completing the recently published N.A. SEMI Proposed RFID Air Protocol Specification. He has authored numerous technical articles, test methods, international round robin tests and related research reports.

**Stephen Chelstrom** received his BSIE from the University of Arkansas at Fayetteville and has been working in the Semiconductor Industry for 24 years. He has worked for Intel, Sematech, Motorola and currently works for Freescale Semiconductor. Automation and system integration has been his primary focus for the last 15 years and he has been a strong proponent of standards for equipment communication and performance monitoring. He is currently moving Freescale towards elimination of the wafer inking process by providing systems that utilize the latest SEMI standards for inkless wafermaps.

**Aidan Cunningham** is applications and marketing manager for wafer marking systems at GSI Lumonics. He has 16 years' experience in the development and implementation of laser marking systems for silicon wafer and IC package traceability in the semiconductor industry.

**Andre van de Geijn** has been working in the semiconductor business for 12 years. He started as an IC designer at IBM. Followed by doing project management on complex video processing IC projects. Most recently he has moved into factory automation in the role of IT architect for the Philips Semiconductors back end process. In this role he is responsible for enabling the smooth introduction of new products by applying state of the art IT in the semiconductor back end process.

Andre got his Bachelor degree in Electronic Computer Integrated Manufacturing in 1993 at the University of Eindhoven the Netherlands. He got his Master degree in Information Technology in 2003 at the Open University Heerlen the Netherlands. Thesis of this degree was Synergy between central and de-central development of process IT, in a global production network: how the Open Source way of working and technologies can be used in an Inner Source way.

**Dave Huntley** is the founder and president of KINESYS Software since 1992 with responsibility for software architecture, strategic marketing and business development. He has been involved with the development and marketing of the Assembly Line Production Supervisor (ALPS) product line.

Dave has been involved with standards development since 1989. He is currently the co-chairman of the Sort Map task force at SEMI responsible for the Substrate Mapping standards (SEMI E142) for final manufacturing.

Dave received a first class honours degree in Electrical and Electronic Engineering from Bristol University, UK.
Biographies of presenters (cont’d)

Josef Pfaffinger joined Rofin-Sinar Laser in 1984. Prior to taking over the software development group for the semiconductor industry in 1995, he has been involved with project management and software architecture. The years of experience in the field of software engineering focused on design and development of communication processes and application programming interfaces. Since 2002 he is responsible for the Rofin software department.

Josef Pfaffinger got a technical degree in electronic engineering in 1984 and a diploma in applied computer science in 1998 from AKAD University/Germany.
Introduction to the SEMI E142 Standard

By: Dave Huntley – Kinesys Software

Abstract:
This presentation will introduce the topics covered by the E142 standard and the requirements that the Sort Map task force strove to meet in its development. The structure of the document suite and its relationship to other standards will be discussed and a few simple examples of its application given. The intention is to provide a background and overview to set the stage for the rest of the program.

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Introduction to the E142 Standard

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Substrate Mapping Overview

- Inspection
- Wafer Probe
- Die Attach
- Wire Bond
- Strip Test
- Laser mark Singulation

Mapping
- Wafers
- Strips
- Trays

Tracking
- Substrate Device

Image Courtesy of KINESYS Software, 2004
Substrate Mapping Standards
XML Schema (E142.1)

- Maps Object Model (UML) to an XML Schema
SECS II Protocol (E142.2)

- Allows equipment to download and upload substrate (wafer, strip, tray) maps (bin code, transfer, device id) via a SECS/GEM interface.
Web Services (E142.3)

• Allows direct, secure, reliable transfer of substrate maps
Substrate Types

- **Wafer Types**
  - Small die
  - Reticle shot map
  - Multi-project
  - Bumped wafers

- **Strip Types**
  - Multi-chip
  - Stacked

- **Tray Types**
  - JEDEC
  - Burn-in
Participants

- The SEMI E142 Substrate Mapping standard was developed and reviewed by 40 engineers from 13 end user and 8 equipment vendors.
- The Sort Map TF would like to thank in particular the following end users for their participation:
  - Freescale
  - Infineon
  - Philips
  - STMicroelectronics
  - TSMC
Balloting Schedule

• SEMI E142 Substrate Mapping (Approved Oct 2004)
    • SEMI E142.2 SECS II Protocol for Substrate Mapping (July 2005)
    • SEMI E142.3 Web Services for Substrate Mapping (October 2005)
For more information

• SEMI Information and Control Committee
  – Paul Trio (ptrio@semi.org)
  – Sort Map TF
    • Meeting room
      http://teams.semi.org/QuickPlace/standards/icsortmaptf/
      Main.nsf/
    • Chairman Dave Huntley
      (dave.huntley@kinesyssoftware.com)
Implementing E142: A Case Study

By: Steve Chelstrom – Freescale Semiconductor

Abstract:
Freescale will share their experiences with the implementation of the SEMI E142 Substrate Mapping standard and a system overview of their components. The current manufacturing environment that is driving the standard and the benefits will be discussed. A description of the tools that are available to the industry for implementing the E142 standard will be presented. Freescale will discuss further enhancements to the standard to improve the transfer of inkless wafer maps between internal and external manufacturing sites and what probe and test suppliers could provide to further improve their products for IC manufacturing.

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Implementing E142
A Case Study

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Overview

• Current manufacturing environment at Freescale
• Benefits of the E142 standard
• E142 qualification process with external suppliers
• Some tools for implementation of the standard
• What’s next with E142 in Freescale?
Manufacturing Environment

- Free scale fab/probe sites located in Texas, Arizona, France, Scotland and Japan.
- Freescale Assembly sites in Malaysia and China
- External and joint venture fab/probe sites in France, China and US.
- External assembly sites in US, Korea, Philippines, Malaysia
- Expected increase in the number of external probe and assembly sites used for manufacturing
Probe to Assembly Flow
Why SEMI E142 & Inkless?

• BENEFITS
  – SEMI Standard Format: We are unable to support multiple inkless wafer formats with so many internal and external suppliers.
  – Inkless wafers increase yield and decrease scrap
  – Inking for 300 mm is not supported by the industry and very high die count (80k/wafer) wafers are difficult to ink.
  – SEMI E142 supports multiple devices and references on a wafer and provides necessary building blocks for implementing the standard and mapping wafer maps to your database.
  – SEMI E142 provides a future migration strategy from ftp transfer of wafer maps to using web services.
External Assembly Qualification Process

- SEMI E142 wafer maps are provided to the assembly site.
- Initial Qualification: Three 25 wafer lots picked without error.
- Second Product Qualification: One 25 wafer lot picked without error.
- Monitor assembly pick accuracy via random skeleton requests. Acceptable criteria: Failure rate of 1 per 1200 wafers.
Freescale E142 Product Startup in Assembly Site

Lot 1
Previously Qualified on SEMI E142 MAPS (1 Lot no errors)

Lot 2
Not Qualified on SEMI E142 MAPS (3 Lots no errors)

Lot 3

Pick 1 Wafer Verify Skeleton
Corrective Action
Good
Bad

Pick 3 Wafer Verify Skeleton
Corrective Action
Good
Bad

Pick 5 Wafer Verify Skeleton
Corrective Action
Good
Bad

Pick 5 Wafer Verify Skeleton
Corrective Action
Good
Bad

Pick 5 Wafer Verify Skeleton
Corrective Action
Good
Bad

Pick 5 Wafer Verify Skeleton
Corrective Action
Good
Bad
Implementing SEMI E142

• **Requirements** – 2 months
  – Migrate existing internal system to SEMI E142
  – Provide enhanced viewing and analysis capabilities

• **Design** – 2 months
  – Identify development tools
  – User scenarios and class diagrams
  – High level architecture

• **Code and test** – 4 months
  – Tool selection and training
  – Code development
  – Integration test with current system
  – Production release
Implementation Lessons

• Freeware tools are powerful however:
  – Some features will not work and can set you back weeks
  – New releases of freeware or purchased software can cause things that worked before to break.

• Deployment takes longer than it should
  – Resistance by the factories to move to inkless
  – Any changes or new releases require a major effort to get all internal and external sites upgraded.
  – Each site has a different target platform for your application.

• Software development
  – Don’t rush to coding – get the requirements and design well understood
  – Make sure to have a quick and easy release process so you don’t put the factory down.
  – Setup a new release test environment for your users and have a migration plan for your upgrade.
  – Have at least two dedicated experienced developers for the project or consider contract help and buying the application.
SEMI E142 System (EWM)

Freescale Internal PROBE

- KLA INF or PRO CIM
- Promis
- Wafer Completed File & Ship To
- EWM WEB Application
- EWM Map-Defect Database
- DBOX XFER
- External Assembly FTP Site SEMI E142
- DBOX XFER
- PROBE FTP Site SEMI E142

Freescale Internal Assembly

- KLM Genesis MES Database
- BAT 3 Genesis MES Database
- ATX TABLE LOADER
- Austin TEST DSA Database Tables
Tools

- SEMI E142 and the sub documents provide definitions for the standard and the schema document (E142-1-V0105-Schema.xsd).
- Several tools will read the schema document and generate code which will provide a starting point for your SEMI E142 inkless application:
  - Java Architecture for XML Binding (JAXB)
  - Castor XML mapping
  - JSQLMapper
  - XSD Schemas for VB Developers
    [http://www.developerfusion.co.uk/show/2386/](http://www.developerfusion.co.uk/show/2386/)
  - Microsoft SQLXML 3.0
- If building a system internally Freescale recommends starting with an xsd tool and not modifying an internal parsing tool that just reads the xml file and pulls out the map.
- **ALPS 3** from Kinesys Software offers fully E142 compliant data management, factory-to-factory transfer and equipment integration for wafer sort, assembly and test.
What’s Next

• Elimination of ftp transfer of wafer maps (push system) to a web service style of wafer map pull system.
• Increase integration with visual inspection tools, MES and planning systems to reduce user interaction required to provide SEMI E142 maps to assembly sites.
• Provide wafer probe and reticle configurations to engineering analysis systems.
• Improved viewing, data storage and retrieval of SEMI E142 wafer maps
• Continue to engage with our external partners to move to the SEMI E142 standard.
• Improve our reference locations on our wafers and continue to migrate our products to inkless.
Extending the Scope of E142

By: Andre van der Geijn – Philips Semiconductor

Abstract:
The SEMI E142 scope statement says that it… “applies to the substrate types; wafers, frames, strips and trays… for assembly and packaging including the testing of semiconductor devices.”.

SEMI E142 does indeed address the representation and storage of substrate information in a structured way for these purposes, but it turns out that it can be applied beyond the initially intended scope. When the E142 object model is mastered, it helps to think “out of the box”, and consider what else can be done with it.

In this presentation we want to show how the object model can be used to:
1. Exchange reticle information with foundries
2. Provide a graphic representation of the map to the operator
3. Offer a modular interface that can support plug and play analysis modules
4. Use of those analysis modules at the subcontractor site, so they can act as they were an in house supplier, making it easy to balance load between subcontractors, without loosing functionality.

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The SEMI E142 Object Model: Extending the Scope

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Who am I?

• I’m the Information Architect of the test and assembly factories of Philips Semiconductors

• I’m the person who get questions like:
  – Can you send maps of subcons to our die attacher?
  – Can you send maps of our testers to subcons?
  – Can you provide the same analysis tools we have in house to our subcons without losing IP?
  – We are going to have stripmaps, what 2D label can we use?
  – We need a copy of the wafer maps for our equipment analysis?
  – Why does it always take such a long time to get working software…..
Who do I want to be?

• THE Information Architect of the test and assembly factories of Philips Semiconductors

• THE person who gives solutions like:
  – You can send maps of the subcons to any equipment
  – You can use a webservices to send automatically maps to subcons
  – Subcons can send maps via webservices to our server, we run the analysis, and the subcon can see the results by a web interface
  – 2D codes are a SEMI T9 standard, and yes we can store the maps
  – Your equipment analysis tool can access the maps via libraries
  – We have one SW package based on a well-considered object model giving all the solutions today …..
SEMIE142

- The SEMI E142 scope statement says that it…”applies to the substrate types; wafers, frames, strips and trays… for assembly and packaging including the testing of semiconductor devices.”.

- SEMI E142 does indeed address the representation and storage of substrate information in a structured way for these purposes, but it turns out that it can be applied beyond the initially intended scope. When the E142 object model is mastered, it helps to think “out of the box”, and consider what else can be done with it.
How to master the E142 object?
How to master the E142 object?

It is embedded in our software = 1:1 relation

Levels of object model

Attributes of the levels

```cpp
// Forward declarations
TSMDDevice = class;
TSMDDeviceMap = class;
TSMDDeviceSubstrate = class;
TSMDDeviceLogicalCoordinates = class;
TSMDDeviceXYDimensions = class;
TSMDDeviceZDimensions = class;
TSMDDeviceOverlay = class;

{ Layout class }
TSMDDeviceLayout = class (TObject)
private
  FLayoutId: string;
  FDefaultUnits: string;
  ChildLayouts: TStringList; //list of names
  FTopLevel: boolean;
  FTopImage: string;
  FBottomImage: string;
  FProduct Id: string;
  Dimension: TSMDDeviceLogicalCoordinates;
  DeviceSize: TSMDDeviceXYDimensions;
  LowerLeft: TSMDDeviceXYDimensions;
  Height: TSMDDeviceZDimensions;

public
  {attributes of a layout as properties }

//BinCodeMap: contains a list of bincode objects and a list of bindefinitions
//the bincodes itself are stored as integers. The Bintype property stores
//the original bintype. Ascii bincodes are stored using their ordinal values
// 'A' -> 05 etc.
TSMDDeviceBinType = (btAscii, btHexadecimal, btDecimal, btInteger);
TSMDDeviceBinMap = class (TSMDDeviceOverlay)
private
  BinDefinitions: TObjectList;
  BinCodes: array of array of integer; //size is set in constructor
  FNullBin: integer;
  FBIntype: TSMDDeviceBinType;

procedure InitBinCodesArray(const Value: integer);
procedure SetNullBin(const Value: integer);

public
  property NullBin: integer read FNullBin write SetNullBin;
  property BinType: TSMDDeviceBinType read FBIntype write FBIntype;

procedure SetBinCode(x: integer, y: integer; bincode: integer); overload; //x, y coordinates
procedure SetBinCode(x: integer, y: integer; bincode: char); overload;
function GetBinCode(x: integer, y: integer): integer;
```
Out of the Box

- Reticle Layout
- Modular analysis
- Operator Gui
- Subcon interface
Reticle layout: the picture
Reticle layout: object model

- **Wafer, reticle & die layout**
- **Reticle positions**
- **Die quality & bin definitions: Die to test**
- **PCM Ugly Test**
- **Relations between layout and die/bin**
- **Border & product info**
- **Enabler for tracking relation between die and reticle**

Diagram:
- Layout -> SubstrateMaps -> Substrates
- Layout -> ChildLayout
- ReferenceDevice -> ReferenceDevices
- Overlay
- BinDefinition
- BinCode
- BinCodes
- BinCodeMap
- DeviceMap
- DeviceIds
- TransferMap
- Transfer
- Aliases
- Substrate

STEP: E142 Substrate Mapping and Device Traceability - Extending the scope - Andre van de Geijn – Philips Semiconductor
Reticle layout: XML-ized
Reticle layout: conclusion

As the reticle layout information fits into the E142 object model & the object model is implemented in SW as it is described in the standard = easy to extend the E142 to this area
Operator GUI: the picture

Browsable Lot & wafer relation

Will be extended by:
- prober
- product Etc.

Bin description and count info
Operator GUI: the picture of MTBF

Next integration step will be here

Lot - wafer relation. From SEMI Object DB

Tester - Prober relation

Integrated tractability for MTBF
Operator GUI: the Web picture

Any place, any where

Layout + bin info

Stripmap

Access to map info: size, flat info quadrants, etc.

Access to prober info: proberID, probecardID, etc.

Bin description and count info
Operator GUI: object model

- Support of wafermaps and stripmaps
- Map Creator: ProberID
- Bin description and count info
- ProberID, probecardID
- WaferID
- Bin description and count info

Diagram:
- MapData
  - Layout
    - ChildLayout
      - 0..* Layout
  - SubstrateMap
    - Overlays
      - 1..* Overlay
        - ReferenceDevice
          - 0..* ReferenceDevices
            - 1 BinDefinitions
              - 0..* BinDefinition
                - 1 BinCodeMap
                  - 1 BinCodes
                    - 1..* BinCode
                      - 1 SubstrateMaps
                        - 1 Substrates
                          - 1 Substrate
                            - 1 Aliases
                              - 0..* AliasId
                                - 1 ProberID
                                  - 0..* probecardID
                                    - 1 WaferID
                      - 1 DeviceIds
                        - 1 Deviceld
                          - 1 Transfers
                            - 1 Transfer
Operator GUI: interface API

```java
package OperatorGUI;

public class OperatorGUI {
    private String SubstrateID;
    private String LotID;
    private String SiteName;
    private String TestStartTime;
    private String TestEndTime;
    private String TestSystem;
    private String Status;
    private int MapIndexID;

    public OperatorGUI() {
        // Initialize attributes
    }

    public void FillResults() {
        // Fill results
    }

    public void MakeE142AttributesAvailable() {
        // Make E142 attributes available
    }

    public void ProvideE142AttributesInAnInterface() {
        // Provide E142 attributes in an interface
    }

    public void UseTheAttributesInOtherApplications() {
        // Use the attributes in other applications
    }

    public static void main(String[] args) {
        if (dbConnection.CheckConnection() != DBReconnect.dbError) {
            QoSelectMap = new QoSelectMapClass();
            QoSelectMap.Find(string.Empty, string.Empty, string.Empty, now, now);
            while (!QoSelectMap.EOF()) {
                myLots.Rows.Add(new object[]{QoSelectMap.LotID, QoSelectMap.SubstrateID});
                QoSelectMap.Next();
            }
        }
    }
}
```
Operator GUI: conclusion

As the substrate information is stored in the E142 object model & the object model is made available as an interface in the SW = easy to make substrate info available for (other) applications
Modular interface: data-input

Collect the data from any resource and store it into the Semi object
Modular interface: resources

Manage resources:
The entities who provide and use data
Modular interface: modules

Create modules and assign actions
Modular interface: data-output

The resource assigns its data to a module, by using the object model. The module takes it action on the object model, and sends it to the correct output.
Modular interface: object model

Data-input resource

Object in memory

Merge
- bump, edit, partials

Cluster detection

Limit check

Yield analysis
- RRR, stacking, reticle layout

DB

Shop Floor control

Modules connected to memory

Modules send data

STEP: E142 Substrate Mapping and Device Traceability - Extending the scope - Andre van de Geijn – Philips Semiconductor
Modular interface: example

**Reliability Improvement and Burn In Optimization through the Use of Die Level Predictive Modeling**

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**Figure 3:** Groupings of nearest neighbor die used in the discriminant analysis. A group consists of all die with a given number or lower, and the number is the number of die in the group. See the text for detailed explanation.

**Figure 9:** Near optimum weights for die in center portion of tester using the algorithm described in the text. Note that the die at the lower left of the focal region is a “region 1” die and so has its weighting coefficient reduced compared to the normal generic coefficients. See the algorithm description in text.
Modular interface: example
Modular interface: the code

```java
Function TakeDieIntoAccount(aBinDefinition : IBinDefinition) : boolean;
procedure DetermineEdgeBies(aBinCodeMap : IBinCodeMap);
procedure DetermineRegionMatrix;
function DetermineNeighboringBies(aX, aY : integer) : TCollection;
protected
public
constructor Create;
destructor Destroy; override;

property Weight1 : double read FWeight1 write FWeight1;
property Weight2 : double read FWeight2 write FWeight2;
property Weight3 : double read FWeight3 write FWeight3;

function DetermineLocalYield(aSemMapData : ISemMapData) : TResultArray;
function DetermineULPY(aSemMapData : TInterfaceList) : TList;
function AnalyzeMaps(aSemMapData : TInterfaceList; aULPYScrapLimit : double;
aScrapBin : integer; aMaxYieldLoss : double) : TInterfaceList;
```

For `i := 0 to aNeighbors.Count-1 do`
begin
  `aNeighbor := aNeighbors.Items[i] as TNeighbor;`
  `iCheckBin := aBinCodeMap.GetBinCode(aNeighbor.X, aNeighbor.Y);`
  `aBinDefinition := aBinCodeMap.GetBinDefinitionByCode(iCheckBin);`
  if `TakeDieIntoAccount(aBinDefinition)` then
    begin
      `dWeight := dWeight + aNeighbor.Weight;`
      if `aBinDefinition.Pick` then
        `dScore := dScore + aNeighbor.Weight;`
    end;
end;
```
Modular interface: conclusion

As the substrate information is stored in the E142 object model in memory &
it can be accessed by uniform SW API modules

= easy to develop new modules
easy to take them fast into production
Subcon interface

- Processes done by subcons is growing:
  - Bumping
  - Embedded IC in smart cards
  - Naked die delivery
  - System in package

- Our internal customers are asking the same analysis functionality we have in house, to be available at subcontractors: the modules
Subcon interface: the picture

Subcon

Maps

Analysis

Philips

E142 Object Model SW

DB

Modules

Webservice

Web GUI

STEP: E142 Substrate Mapping and Device Traceability - Extending the scope - Andre van de Geijn – Philips Semiconductor
Subcon interface: scenario

- Subcon delivers maps in E142 webservice
- Data-input read maps into memory and DB
- Module analysis map in memory
- Updated map are send back to subcon via webservice
- Results of analysis are made visible by Web
- Subcon WoW equals in house activity
- IP of modules can stay in house
Conclusion

- The E142 standard not only solves working with all different kind of maps
- It helps in thinking in an object way, which can be used to brings solutions to the area around it
- Solutions which are provided fast to production & customers
- And which can work together

With E142 you can focus on the process etc, you know that the object as the backbone is capable in supporting you
SEMI E142 Map and Process Examples

By: Dave Huntley – Kinesys Software

Abstract:
Some examples will be given showing how complex devices (e.g. stacked SiP, multi-project wafers, etc.) may be mapped with E142. This will be followed by some examples of process flows in which E142 can facilitate the feed forward and feed back of bin code maps and device level traceability data.

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E142 Map and Process Examples

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Introduction

• Map Examples
  – Bin Code Maps for…
    • Stacked Package
    • Multi-project Wafer (MPW)
  – Transfer Map
  – Deviceld Map

• Application Areas
  – Wafer sort
  – Assembly and test
    • Singulated Test
    • Strip test
Stacked Package Maps

<SubstrateMaps>
  <SubstrateMap SubstrateId="Strip-1000023" SubstrateType="Strip" LayoutSpecifier="Strip/DeviceLocations">
    <Overlay MapName="Bare strip test result" MapVersion="1">
      <BinCodeMap BinType="Decimal" NullBin="0">
        <BinDefinitions>
          <BinDefinition BinCode="005" BinDescription="Good device location"/>
          <BinDefinition BinCode="115" BinDescription="Bad device location"/>
        </BinDefinitions>
      </BinCodeMap>
    </Overlay>
  </SubstrateMap>
  <SubstrateMap SubstrateId="Strip-1000023" SubstrateType="Strip" LayoutSpecifier="Strip/DeviceLocations/FlipChipDevices">
    <Overlay MapName="Flip Chip dies" MapVersion="1">
      <BinCodeMap BinType="Decimal" NullBin="0">
        <BinDefinitions>
          <BinDefinition BinCode="032" BinDescription="Pass dies"/>
          <BinDefinition BinCode="185" BinDescription="Reject dies"/>
        </BinDefinitions>
      </BinCodeMap>
    </Overlay>
  </SubstrateMap>
  <SubstrateMap SubstrateId="Strip-1000023" SubstrateType="Strip" LayoutSpecifier="Strip/DeviceLocations/WireBondDevices">
    <Overlay MapName="Wire Bond dies" MapVersion="1">
      <BinCodeMap BinType="Decimal" NullBin="0">
        <BinDefinitions>
          <BinDefinition BinCode="035" BinDescription="Pass dies"/>
          <BinDefinition BinCode="186" BinDescription="Reject dies"/>
        </BinDefinitions>
      </BinCodeMap>
    </Overlay>
  </SubstrateMap>
</SubstrateMaps>
Multi-project Wafer

<Layout LayoutId="WaferLayout" DefaultUnits="mm">
  <Dimension X="1" Y="1" />
  <DeviceSize X="300.000" Y="300.000" />
  <LowerLeft X="10.000" Y="10.000" />
  <TopImage>Images\w300.jpg</TopImage>
  <ChildLayouts>
    <ChildLayout LayoutId="DeviceGroups" />
  </ChildLayouts>
</Layout>

<Layout LayoutId="DeviceGroups" DefaultUnits="mm">
  <Dimension X="20" Y="12" />
  <DeviceSize X="15.000" Y="25.000" />
  <StepSize X="15.000" Y="25.000" />
  <LowerLeft X="5.000" Y="6.000" />
  <ChildLayouts>
    <ChildLayout LayoutId="Devices-1" />
    <ChildLayout LayoutId="Devices-2" />
  </ChildLayouts>
</Layout>

<Layout LayoutId="Devices-1" DefaultUnits="mm">
  <Dimension X="3" Y="2" />
  <LowerLeft X="0.200" Y="0.200" />
  <StepSize X="5.000" Y="5.000" />
  <DeviceSize X="5.000" Y="5.000" />
</Layout>

<Layout LayoutId="Devices-2" DefaultUnits="mm">
  <Dimension X="1" Y="1" />
  <LowerLeft X="0.200" Y="10.200" />
  <DeviceSize X="15.000" Y="15.000" />
</Layout>
Multi-project Wafer Maps

<SubstrateMaps>
  <SubstrateMap SubstrateType="Wafer" SubstrateId="12345-17" LayoutSpecifier="WaferLayout/DeviceGroups/Devices-1" Orientation="0" OriginLocation="LowerLeft" >
    <Overlay MapName="Small dies" MapVersion="1" >
      <BinCodeMap BinType="Decimal" NullBin="0">
        <BinDefinitions>
          <BinDefinition BinCode="11" BinDescription="Pass die"/>
          <BinDefinition BinCode="22" BinDescription="Fail die"/>
        </BinDefinitions>
        <BinCode>000000000000000000000000000000000000000000000000000000000000000</BinCode>
        <BinCode>000000000000000000000000000000000000000000000000000000000000000</BinCode>
        <BinCode>000000000000000000000000000000000000000000000000000000000000000</BinCode>
        <BinCode>000000000000000000000000000000000000000000000000000000000000000</BinCode>
        <BinCode>000000000000000000000000000000000000000000000000000000000000000</BinCode>
        ...
      </BinCodeMap>
    </Overlay>
  </SubstrateMap>
  <SubstrateMap SubstrateType="Wafer" SubstrateId="12345-17" LayoutSpecifier="WaferLayout/DeviceGroups/Devices-2" Orientation="0" OriginLocation="LowerLeft" >
    <Overlay MapName="Large dies" MapVersion="1" >
      <BinCodeMap BinType="Decimal" NullBin="0">
        <BinDefinitions>
          <BinDefinition BinCode="11" BinDescription="Pass die"/>
          <BinDefinition BinCode="22" BinDescription="Fail die"/>
        </BinDefinitions>
        <BinCode>000000000000000000000000000000000000000000000000000000000000000</BinCode>
        <BinCode>000000000000000000000000000000000000000000000000000000000000000</BinCode>
        <BinCode>000000000000000000000000000000000000000000000000000000000000000</BinCode>
        <BinCode>000000000000000000000000000000000000000000000000000000000000000</BinCode>
        <BinCode>000000000000000000000000000000000000000000000000000000000000000</BinCode>
        ...
      </BinCodeMap>
    </Overlay>
  </SubstrateMap>
</SubstrateMaps>
Transfer Map

```xml
<SubstrateMap SubstrateType="Strip" SubstrateId="RS_Strip2"
            LayoutSpecifier="RS_StripLayout2/RS_SRAM2">  
  <Overlay MapName="WaferToStrip" MapVersion="1">
    <TransferMap FromSubstrateType="Wafer" FromSubstrateId="Wafer1">
      <T FX="12" FY="12" TX="0" TY="0"/>
      <T FX="13" FY="12" TX="0" TY="1"/>
      <T FX="14" FY="12" TX="0" TY="2"/>
      <T FX="15" FY="12" TX="1" TY="0"/>
      <T FX="16" FY="12" TX="1" TY="1"/>
      <T FX="17" FY="12" TX="1" TY="2"/>
      <T FX="18" FY="12" TX="2" TY="0"/>
      <T FX="19" FY="12" TX="2" TY="1"/>
      <T FX="20" FY="12" TX="2" TY="2"/>
      <T FX="21" FY="12" TX="3" TY="0"/>
      <T FX="22" FY="12" TX="3" TY="1"/>
      <T FX="23" FY="12" TX="3" TY="2"/>
    </TransferMap>
  </Overlay>
</SubstrateMap>
```
DeviceId Map

<SubstrateMap SubstrateType="Strip" SubstrateId="RS_Strip_23"
    LayoutSpecifier="/RS_StripLayout_23/RS_SRAM_23"
    Orientation="0" OriginLocation="LowerLeft">
    <Overlay MapName="2D Matrix" MapVersion="1">
        <DeviceIdMap>
            <Id X="0" Y="0">LOT001-1</Id>
            <Id X="1" Y="0">LOT001-2</Id>
            <Id X="2" Y="0">LOT001-3</Id>
            <Id X="3" Y="0">LOT001-4</Id>
            <Id X="4" Y="0">LOT001-5</Id>
            <Id X="5" Y="0">LOT001-6</Id>
            <Id X="6" Y="0">LOT001-7</Id>
            <Id X="7" Y="0">LOT001-8</Id>
            <Id X="8" Y="0">LOT001-9</Id>
            <Id X="9" Y="0">LOT001-10</Id>
            <Id X="0" Y="1">LOT001-11</Id>
            <Id X="1" Y="1">LOT001-12</Id>
            <Id X="2" Y="1">LOT001-13</Id>
            <Id X="3" Y="1">LOT001-14</Id>
            <Id X="4" Y="1">LOT001-15</Id>
            <Id X="5" Y="1">LOT001-16</Id>
            <Id X="6" Y="1">LOT001-17</Id>
            <Id X="7" Y="1">LOT001-18</Id>
            <Id X="8" Y="1">LOT001-19</Id>
            <Id X="9" Y="1">LOT001-20</Id>
            <Id X="0" Y="2">LOT001-21</Id>
            <Id X="1" Y="2">LOT001-22</Id>
            <Id X="2" Y="2">LOT001-23</Id>
            <Id X="3" Y="2">LOT001-24</Id>
            <Id X="4" Y="2">LOT001-25</Id>
            <Id X="5" Y="2">LOT001-26</Id>
            <Id X="6" Y="2">LOT001-27</Id>
            <Id X="7" Y="2">LOT001-28</Id>
            <Id X="8" Y="2">LOT001-29</Id>
            <Id X="9" Y="2">LOT001-30</Id>
        </DeviceIdMap>
    </Overlay>
</SubstrateMap>
Application Areas

• Wafer Sort
  – Collecting map data from equipment
  – Substrate traceability
  – View, edit, analyze map data

• Secure Transfer
  – Site to site transfer of map data
  – SEMI E142 Web Services

• Assembly and Test
  – Deliver map data to equipment
  – Substrate traceability
  – Device traceability
  – Singulated test
  – Strip test
Wafer Sort
Secure Transfer

- No lost maps!
- Fast transfer
- Sensitive data encrypted
- Non-repudiation
  - Sender and receiver can prove transaction occurred
Assembly & Test Example 1
Assembly & Test Example 2
Test Data Feedback

- Rebuild wafer maps from final test
- Connect final test to inspection & test in wafer fab
- Identify process problems
- Improve yield
- Provide instant device tracking reports
Wafer Level Die Marking and E142

By: Aidan Cunningham – GSI Lumonics

Abstract:
GSI Lumonics supplies laser systems used for IC traceability and product identification marking. We will discuss the emergence of IC marking for traceability as a wafer level process by back end packaging services.

New requirements for marking have emerged during the last two years as result of bare die applications finally becoming mainstream. The demand by consumer electronics for the low pin count bare die found in cell phones, PDA’s, FPD’s, Digital cameras has necessitated new equipment be developed to mark the higher value die prior to singulation.

Critical issues for integrated device manufacturers (IDMs) and outsourced packaging suppliers are the management and control of marking information and substrate mapping data. The IDM must be certain that accurate information is encoded onto the backside of the bare die for product ID, time/date stamp, lot ID, Pin one orientation, etc.

The issue is traceability to the fab front end production process all the way back to the particular row and column on the wafer. This task could be greatly simplified with the implementation of the E 142 standard resulting in benefits for both tool supplier and IC manufacturer. We will present examples of how cost and lead times could be reduced while production flexibility enhanced with the implementation of SEMI E142 standard.

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Wafer Level Die Marking
and
SEMI E142

Aidan Cunningham
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Overview

- Need for Traceability
- Changes in Packaging Technology
- Wafer Level Die Marking
- Traceability Requirements
- Extending Back End Marking Process
- Solutions with Existing Technology
Drivers for Traceability

- Growth of foundry services and outsourcing
- Vendor to vendor tracking
- Accountability and liability for manufacturer and consumer
- Increasing complexity of devices and packaging
- Process monitoring
  - quality control
  - minimize rework
- Reduce test cycle, rework and time to market
- Field recalls and returns

A consistent and reliable means of reporting, storing and transmitting substrate map data is required.
What’s Driving the Need for CSP?

Reduced package size
- System on Chip (SOC)
- Stacked die packaging
- High value, high performance packages

Driven by
- Cell phones
- Consumer electronics
- Flat panel displays
- Small portable wireless devices
Driven by Consumer Products

Display Board

- 3 Chip BGA
  - Wire Bonded
  - 8.3x9.6x1.4 mm
  - 72 connects

2 Chip BGA
- Wire Bonded
- 14x13x1.4 mm
- 134 connects

Main Board

- Double Sided FC-BGA
  - Baseband and Application Processor

- Stacked BGA Package
  - Flash and DRAM

- Dual Chip BGA
  - Video Processor
  - Flip Chip and Wire bond

- 11 CSP or Flip Chip devices

- Multiple wafer sources

- Traceability is critical

- Mark die at wafer level

- **SEMI E142 will reduce tooling and handling cost at every step**
Traditional IC Marking Requirements

- Plastic or ceramic
- Ink and laser marked
- Laser preferred for cleanliness
- Pin one molded into package
- Typical mark
  - Lot Number
  - Date Code
  - Company Logo
- Back-end process
- Traceability to lot only!!!!
Wafer Level Die Marking Application

**Industry Applications**
- Primarily back-ground silicon for bare die, CSP packaging
- < 1um depth
- die sizes < 1mm to 8mm range
- > 300um wafer thickness
- Often bumped wafers
Wafer Level Die Marking Application

Marking Characteristics
- 1 to 5 µm depth
- Multiple wafer surface finishes
- Back-ground, oxidized, epoxy, gold
- Treats wafer as substrate

GSI Lumonics Expertise
- Laser Design
- Beam Steering Technology
- Beam Alignment Accuracy
- System Level Integration
Wafer Level Die Marking Requirements

**Permanent Mark**
- Product ID / Part #
- Pin one Orientation
- Logo
- Date Code
- Bin Code
- Serialization
- Traceability to row/column ingot, cassette, etc.

**How E 142 Standard will Help**
- Data is encompassed within E142 standard
- No need to reinvent the wheel for every customer
- Custom software minimized
- Lead time is reduced
Wafer Level Marking – Cost Effective

- Wafer level packaging drives all processes to be completed before singulation – *including identification marking!*
- Avoids the cost of handling singulated die after test
- Improves factory throughput
- Ideal application of substrate mapping standards to further reduce costs
Existing Traceability Methods

- **Wafer ID marking**
  - 20 years
  - Laser based
  - Semi standards apply
    - (SEMI OCR, M12, M13, T1, T7 and more)
  - Traceability from ingot through fab
  - Front-end process silicon supplier and fab

- **Singulated Package Marking**
  - Ink and laser
  - Lot, Date Code and Device Identification
  - Handling difficult for CSP and very small parts
  - Environmental concerns
  - Back-end process
Opportunity for Continuity in Traceability

QFP, BGA, Flip Chip

Wafer → Dicing → Packaging

Wafer Level CSP

Wafer → Dicing → Packaging

STEP: E142 Substrate Mapping and Device Traceability – Wafer Level Die Marking - Aidan Cunningham, GSI Lumonics
Ingot

**Hard mark**
Cut Wafers
Before Chemical
Etch and Polish
Silicon Supplier

**Soft Mark**
FAB Process

**Die Mark**
Wafer Level
Back End

**Problem**
- Dicing destroys die traceability below the lot level
- Individual die cannot be traced to the source wafer
- Individual die cannot be traced to their wafer location
- Wafer level die marking maintains traceability down to the row and column level on the wafer
- No gap in traceability
- Requires access to substrate map at every step
How do you mark these die?

- 8” wafer
- 2mm x 2mm die
- 7,500 die per wafer

Marking single die would require thousands of handling steps
# Understanding Die Marking Requirements

## Product Setup

- **Mark Design**: Characters, font, dynamic text label
- **IC and mark orientation**: Superimposing front/back images
- **Wafer geometry**: Row/Column, useable die

## System Setup

- **Vision training**: Wafer ID, wafer alignment pattern, mark inspection

## WIP Management

- **Wafer/Job Association**: Host communication automatic data input
  - Lot ID and Wafer ID job identifiers
  - Minimal operator input

## Quality Control

- **Zero defects**: Integrated mark quality verification
  - Auto laser power monitoring
  - Mark to die alignment checking
  - Auto calibration for power
  - Auto calibration for mark accuracy
Front-end to Back-end continuity

E142 formatted data source

Download wafer map → Load marking job and layout → Mark wafer

Complete traceability back to row, column, slot and ingot guaranteed

Inspect mark and verify wafer ID
Faulty Mark Prevention

Wafer Map Translator
- Multiple formats in use
- Custom software required to import correct wafer geometry and bin information
- Each customer uses unique wafer map format to capture the same information!!
- Some customers forced to use multiple formats

E142 Substrate Map Standard will minimize need for custom software and ensure transfer of accurate mark information
Factory Automation

Link to FA database
- to retrieve wafer map from probers & inspection tools

Central storage
- of common mark job files between systems

Link wafer IDs
- to correct wafer map to assure correct mark data

Adoption of a substrate map standard means systems will “speak the same language”
Mark Orientation

- Wafer level marking requires one alignment sequence using three points.
- The entire wafer can be marked after completing the alignment.
Advantages of Wafer Level Die Marking

- Enables the marking of very small die
- Assures full die traceability to wafer and ingot
- Assures all die have identification marks
- Assures all die have proper orientation marks
- Enables very accurate mark positions on each die
- Enhances mark throughput
Conclusion

✔ Cost effective wafer level die marking systems are available today

✔ Traceability is a key factor for process improvement, cost reduction and quality tracking

✔ Wider adoption of substrate mapping standard such as E142 will reduce costs further for both tool suppliers and IC manufacturers
Laser Marking and SEMI E142

By: Josef Pfaffinger – Rofin Sinar Laser

Abstract:
Rofin Sinar Laser provides laser markers to mark the strip with an ID (2D-Code) onto the surface of the strip. In a second step, strip testing will become more and more important. E.g. automotive electronics manufacturer are a major force behind chip trace ability because vehicle recalls are costing them millions of dollars. Like the wafer map in the front-end the strip map management will improve the back-end automation. From the equipment vendors point of view, the current equipment strip map interface will be discussed. An application scenario will show the integration of laser marker with tester to mark the different bin grades (good or bad) together with device ID maps onto each individual and singulated device. The SEMI Standards are the basic platform for addressing these new requirements.
This presentation will discuss the increasing demand to mark devices with a unique bin-code or device ID and how it can be applied.

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Laser Marking and SEMI E142

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Macro
- Cutting
- Welding
- Surface modification

Micro
- Fine welding
- Fine cutting
- Perforation
- Micro structuring
- Micro drilling

Marking
- Vector/BMP Marking
- Barcode/Data Matrix

Hamburg

Starnberg

Günding
Introduction

• Assembly and Test Example (Dave Huntley)
• SEMI related Software Features
• Substrate Mapping and Marking, How can it be depicted?
• The Integration Aspect, an Application Model
• Applying Strip-ID and BinCodes
• Example: 2D-Code Marking Scenario
• Example: Final BinCode Marking Scenario
• Conclusion
• The End
Assembly and Test Example (Dave Huntley)
SEMI related Software Features

- Matrix Object (for Tray & Strip modeling)
- JEDEC Tray and Leadframe database
- Device-ID and Bin-Code Mapping
- 2D-Matrix code
- Handling Integration Interface
- SECS-GEM / Remote Control
  - Standards: E5 (SECSII), E30 (GEM), E39 (Object Services), E142 (Mapping)
- XML Layout Import / Recipe Download
- Autoteach Interface for Vision Inspection
- Status / Data Logging and Unit-Level-Tracking
Substrate Mapping and Marking, How can it be depicted?

[Image showing a software interface for substrate mapping and marking with Rofin chip marking examples.]
The Integration Aspect, an Application Model

- **Job Data**
  - LOT-File
  - SECS-II - PP-Select
  - TCP/IP Socket
- **Marking Layout**
  - XML-File
  - SECS-II - PP Management

**Bin**
- AssignBin
- SelectBin

**Occupation**
- Job Control
- Recipe Program

**Matrix-Object**
- Cell
  - CellOccupation
  - Dual-Pos.
  - Part

**Handling Control**
- Vision System

**Process Program**
- Process I/O
- Dual-Track
- Part handling
- Occupation
- Bin-Selection
- MultiBin-DataTransfer
- SECS-II - HostCommand
- SECS-II - Map Download
Applying Strip-ID and BinCodes

SEMI E142.1 XML Schema
SEMI E142.2 SECS II Protocol

Non GEM BinMap Formats
TCPIP Commands
PIO-Binning

TCP/IP (HSMS)

SECS/GEM

Equipment Control Software / Custom Application

GetAttr. Request S14,F1
Download Map Data S14,F2
Example: 2D-Code Marking Scenario
Example: Final BinCode Marking

**Diagram: **
- **Cell Controller**
- **RS Controller**
- **Strip-Handler**

**Flowchart Steps:**
- ExternalStartSignal()
- GetStripMap()
- If MAPMODE=1
  - Event "MarkingEnd()"
  - MarkingEndSignal()
- Or
  - S2F41 PP-Select()
- GEM-Var EquipmentMap assigned
- SECI E142.2 SECS II Protocol for Map Download
- Select bins according to EquipmentMap
- Bin1 3GHz
- Bin2 2GHz
- Bin3 failed
- Bin1 3GHz
- Bin2 2GHz
- Bin3 failed
- Bin1 3GHz
- Bin2 2GHz
- Bin3 failed

**XML Code: **
```xml
<xml version="1.0" encoding="utf-8" ?>
<Mapdata xmlns="urn:semi-org:xsd.E142-1">
<Layouts>
  <Layout LayoutId="StripLayout" .....
</Layout>
</Layouts>
<SubstrateMaps>
  <SubstrateMap SubstrateTyp="Strip"
    <BinCode>121321</BinCode>
  </SubstrateMap>
</SubstrateMaps>
</Mapdata>
```

**SEMI E142.1 XML Schema for Substrate Mapping**

**Activate Binning / Assign Layouts:**
- BinCode = 1
  - BinText = "3GHz"
- BinCode = 2
  - BinText = "2GHz"
- BinCode = 3
  - BinText = "failed"

**Additional Notes:**
- **SEMI E142.2 SECS II Protocol for Map Download**
- Select BinCode<121321> for each Device

**Related Documents:**
- **SEMI E142.2 SECS II Protocol for Map Download**
- **SEMI E142.1 XML Schema for Substrate Mapping**
Conclusion

• Today, software projects becomes more complex and the number of dependencies to related systems increases continually, so interface standardisation can reduce engineering work.

• Traceability endpoint is not the fab gate, laser chip code marking work through to the consumer. (Automotive, fair trade etc...)

• Strip & Tray map management will be the driver for future needs in laser marking each device with it's individual map-data while the devices are still mounted on the strip or singulated in trays.
The End

Thank you for your attention!

Questions?
Details on Projects?
Please see us at our booth.
RFID Marking and SEMI E142

By: Winthrop Baylies – BayTech Group

Abstract:
RFID is in the limelight – in Consumer products, DOD shipments and yes, in semiconductor manufacturing. This discussion focuses on RFID’s current role in FEOL processing and its extension to BEOL and Final Manufacturing. RFID Tag / Reader issues and related industry specifications are outlined. Lastly, deployment of RFID tags / readers into Final Manufacturing is explored.

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RFID, Substrate Mapping and SEMI E142

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Outline

- RFID – An Overview
- RFID Elements
  - Tags & Readers
  - Air Protocol / Location
- Message Content
- Device Mapping Issues
- RFID Tradeoffs
- Standards
RFID – In the Limelight

• Consumer - Walmart, . . .
  – Hi-value items - Shelf stock, Inventory Tracking

• Military - DOD
  – Pallet-level Tracing – where is that crate of super-widgets now; how did it get there?

• Semiconductor - 300 mm production
  – FEOL – ALL FOSBs; >95% using RFID
  – BEOL/Probe Test – similar
  – Final Manufacturing – opportunity knocks
RFID – In Distribution

**HOW THE AUTO-ID SYSTEM WILL AUTOMATE THE SUPPLY CHAIN**

With Auto-ID technology, physical objects will have embedded intelligence that will allow them to communicate with each other and with businesses and consumers. Auto-ID technology offers an automated, numeric system of smart objects that revolutionizes the way we manufacture, sell, and buy products. Here’s how it works:

1. **SuperColla, Inc.** adds a Radio Frequency Identification (RFID) tag to every can it produces. Each tag costs about five cents – and contains a unique Electronic Product Code, or EPC. This is stored in the tag’s microcomputer which, at some microsecond, is smaller than a grain of sand. The tag also includes a tiny radio antenna.

2. **These** tags allow the entire case to be identified, counted, and tracked in a completely automated, cost-effective fashion. The cans are packed into cases – which feature their own RFID tags – and loaded onto tagged pallets.

3. **As the pallets of cola leave the manufacturer**, an RFID reader positioned above the loading dock door hits the smart tags with radio waves, so that the cases can be read.

4. **The tags “wake up” and start broadcasting their individual EPCs**. Like a good kindergarten teacher, the reader only allows one tag to talk at a time. It rapidly switches them on and off in sequence, until it’s read them all.

5. **The reader is wired into a computer system running Savant.** It sends Savant the EPCs it’s collected, and Savant goes to work. The system sends a query over the Internet to an Object Name Service (ONS) database, which acts like a reverse telephone directory – it receives a number and produces an address.

6. **This second server uses FPL, a Physical Markup Language, to store comprehensive data about manufacturers’ products.** It recognizes the incoming EPCs as belonging to cans of SuperColla, Inc.’s Cherry Hydro.

7. **Because it knows the location of the reader which sent the query, the system can now also look up other data about the product.** For instance, involving a defect or tampering case, if information would make it easy to track the source of the problem – and recall the products in question.

8. **What’s more**, SpeedyMart’s retail stores also feature integrated readers. When the cans of cola are stacked, the stores “understand” what’s being sold in them. Now, when a customer grabs a six-pack of Cherry Hydro, the distributed shelf will route a message to SpeedyMart’s automated replenishment system – which will order more Cherry Hydro from SuperColla, Inc. With such a system, the need to maintain costly “safety volume” of Cherry Hydro is remote warehouse is eliminated.

9. **As in-aisle makes the customer’s life easier, too. Rather than walk in line for a cashier, she simply walks out the door with her purchases.** A sensor in the door recognizes the items in her cart by their individual EPCs, a couple of the shelf or stack and the customer is on her way.

10. **At home, the refrigerator system** identifies meats to reflect the inventory of Cherry Hydro. As the cola is consumed, the fridge will add the beverage to an automated grocery list.

11. **When the cola cans hit the recycling center, RFID readers will automate the process of sorting them into the appropriate waste category** – eliminating expensive manual sorting. The cans are even ferreted out and their manufacturer far removed from the plant.
Semiconductor Material ID / Transfer

Source: G. Michaud
RFID Elements

- Transponder (Tag) Types
  - Active – battery
  - Passive – reader’s electromagnetic power
  - Read-write vs. Read-only
    - R-W – specialized applications
    - R-only 2 types
      - Encoded during mfg process
      - Changeable – EEPROM
  - Major Variables
    - Message size
    - Operating Frequency
    - Read Range
    - Temperature
    - Size
    - Cost
RFID System Configuration
RFID Elements

- Interrogator (Reader)
  - Many types, sizes, capabilities – matched to fit tag capabilities
  - Powered
  - Direct & remotely activated
- Air Interface – the nitty gritty details
- Tag / Reader Location – “simpler” details
RFID Tag Issues

- Tag Costs – Electronics + Antenna + Package
  - Consumer products
    - Today ~25–50 cents
    - Long-range target ~ 5 cents
  - DOD - higher
  - Semiconductor FOUP - adder
    - $5 – $10

- Challenges
  - Shrink the chip
    - Sawed ~ 1 mm square, 15K / 200 mm wafer
    - Etched ~ 150 µm square, 250K /
  - Handling / Pick-Place
    - Alien Technology – “fluidic self-assembly”
    - Philips – vibratory assembly
  - New antennas
    - Rafsec – hi-speed printing / stamping
  - Si Alternatives
RFID Reader Issues

• Agile Readers
  – Different chip frequencies
  – Anti-collision – TDMA
  – Tag collision – response to selected digits
    • 50 tags / sec

• Read Range
  • Low-freq ~ 4 cm range
  • Hi-freq – longer range, higher reader energy
    – UHF – 3-6 meter read range
Air Interface: 134.2 kHz Systems

- Only 134.2 kHz deployed in 300mm FOUPs
  - Other frequencies / other industries
- Two types of Air Interface
  - Type 1 –
    - Legacy tags, SEMI spec; TI-licensed
    - Legacy readers – only read these tags
  - Type 2
    - New tag types, ISO 18000-2; Other licenses may be required
    - New readers – may read both tag types
Message Example
Electronic Product Code [EPC]

- Unique, Individual-Item, “License Plate”
- Header – EPC version #
- EPC Mgr – typically the manufacturer
- Object Class – Stock Keeping Unit
- S/N – unique to the item
  - 96 bits - 268 million companies / each with 16 million object classes / each with 68 billion serial numbers
BEOL / Final Mfg
Device Mapping Formats/E142

Source: G. Michaud
Device Mapping Issues

• License Plate
  – Unique for ALL devices
  – Small # bytes
  – Compatible with chip location(s)
  – Useful for Complex Devices

• Historical Data
  – Suppliers, Tools, Conditions, Test Results, . .
  – Potentially endless # bytes
  – On-device vs. Archival Data Base
Device Mapping Issues 2

• Complex Devices
  – Multi-device (system on chip)
    • Integral Transponder
    • Antenna
      – Area - e.g. top chip
      – Location – e.g. chip back surface
  • Si Electronics
    – On-chip
      » Back surface or Front surface
    – Dual-side processing
RFID Trade-offs

- **Pros**
  - Not line-of sight
  - Avoids mark-degradation issues
  - Fast read cycle
  - FEOL Experience
  - Open sources
  - Established Stds
    - SEMI, ISO, EPC . .
  - Advancing technology

- **Cons**
  - Antenna area
  - Read range
  - Power source
  - Limited Info-storage
  - Ltd Final Mfg Experience
  - Managing Air Interface across-operations
  - Lack of familiarity
RFID Standards Issues

- **IP / Licenses – 134.2 kHz, HDX-Type Air Interface**
  - Type 1 “Legacy” Tags – TI now licensing
  - Type 2 New Tags – others now licensing

- **SEMI Doc 4110 – open standard, demanded by IC makers**
  - Proposed Std: published June 2005
  - Balloting after SEMICON West 05
  - Details Type 1 Air Interface
    - Lists Type 1 – Type 2 differences (several, important)
      - 6-bit vs 8-bit operation
      - 17 pages R/W memory
      - Pulse Width Modulation, and several others

- **ISO 18000-2**
  - Details Type 2 Air Interface

- **ISO 18000-1, -3, etc.**
  - More Air Interfaces
Selected Marking Standards

• ANSI/EIA
  – 16022 *Intnl Symbology – Data Matrix*
  – 16388 *Automatic ID/Data Capture – Bar Code39*
  – 706 *Component Marking Std* [Data Matrix on Device Packages]
  – 556-B *Outer Shipping Container Labels* [2D, 1D (BC39+HRI) on Labels]
  – 624 *Bar Code Labels* Non-retail Applications
    [Product Packages Distributed Outside Originating Org.]
  – MH10.8.2 *Application Identifiers* [Prefixes that Identify the Meaning/Format of the Data Field that follows the AI]
Selected Marking Standards - 2

- **SEMI Specifications** (-xxxx = Publishing Date; c.f. 0302 = Mar 2002)
  - M12-1103 A/N on Si Wafers (10-character message)
  - M13-1103 A/N on Si Wafers (18-character message)
  - T2-0298 [reapproved 1104] BC-412 on Si Wafer Back-side
  - T3-0302 Wafer Box Labels [Data Matrix, BC39, HRI on (paper) material]
  - T7-0303 Data Matrix, 300 mm Wafer Back-side
    - M1.15-0303 Optional A/N Field, 300 mm Wafer B/S
  - T9-0200 Data Matrix on Lead Frame Strips
  - T10-0701 Assessing Data Matrix Mark Quality
Savant Technology
Network’s Nervous System

- Distributed Architecture
- Data smoothing
- Reader coordination
- Data forwarding
- Data storage
  - Real-time in-memory event database (RIED)
- Task Management System (TMS)
RFID Communications

• Auto-ID Savant Specification 1.0
  – Sits between tag readers and enterprise applications
  – Computational functions for selected applications
  – Sun, UCC, MIT
Savant Overview

Inter-module interaction through APIs defined by specific processing modules

Other Services Used by Specific Processing Modules

User-defined Processing Modules

Standard Processing Modules

Processing Module Container
EPC Network Architecture-inside the Enterprise

- Local copy of frequently used ONS data
- Registration for static and dynamic ONS
- Collaboration on asset tracking

- Track and trace serial items
- Referencing business transactions
- Object type data (e.g., pallet/case/item,...)
- Instance level EPC data (e.g., expiry date,...)
- Fine grained access control policy implementation

- Report data
- Manage readers
- Higher level filters

- Capture events data (tag and sensors)
- Simple filters

- Transmit ePC data using radio frequency
- Transmit sensor data
EPC Network Architecture-across Enterprises

Static ONS:
- Converts an EPC into an internet address to locate EPC Information Service.

Dynamic ONS:
- Provides means to locate current and previous EPC custodians for the purpose of track and trace, recall, etc.

- Web service interface describing the capabilities and data accessible through each EPC Information Service to trading partners.
Object Name Service (ONS)

- ~ Domain Networking Service (DNS)
- When tag is read
  - EPC → Savant → ONS → Savant Server → Product File Info → Co. inventory / supply chain operations
- ONS Special Requirements
  - Local servers
  - Built-in redundancies – crash / data protection
Physical Markup Language

- XML-based
- Universal – describes all
  - Objects – hierarchical; SI and NIST work
  - Processes / Environments
    - Dynamic data
    - Temporal data
- Started simply, will evolve
And Recently:

$15M-25M
2 Years Deployment

$100M/Year
Lost Baggage

25-35 cents
Per Chip

Delta aims to put end to lost luggage

By Bruce Mohl

It’s all in the tag.
Delta Air Lines said yesterday it plans to virtually eliminate the problem of lost luggage by using radio frequency identification technology in baggage tags to track the whereabouts of any bag in its possession.
The Atlanta-based airline said it will take roughly two years and $15 million to $25 million to deploy a radio frequency identification system across its domestic network. But once the job is done, the company said, it will be able to track a bag from the time it is dropped off at check-in until it is delivered to the baggage carousel at the customer’s destination.

“We hope to come as close as we can to eliminating the problem of misplaced baggage,” said Rob Maruster, director of airport strategy, planning, and development at Delta.

While other airlines and airports have experimented with radio frequency identification, or RFID, Delta is the first major carrier to implement plans for widescale deployment.

If the system works effectively, Maruster said, it will not only improve the flying experience of Delta’s passengers, for whom a lost bag can be a defining negative experience, but it will save the airline a lot of money. The company said the decision was not security related.

Delta last year mishandled about four bags for every 1,000 it handled, according to the US Department of Transportation. Maruster said the airline spent approximately $100 million recovering and delivering those mishandled bags to passengers.
The company ran tests of the technology last year and this year on flights between Jacksonville and Atlanta. The most recent test showed the system could track bags 100 percent of the time.

RFID tracking relies on tiny microchips embedded in tags that are attached to passenger bags. The chips enable readers using radio frequencies to identify the tag if it passes within 20 feet. It’s similar to the EZ Pass system used by the Massachusetts Turnpike Authority.

In essence, the system tracks a bag by identifying where it was last seen. Tag readers would be located at the check-in counter, along conveyor belts leading to baggage handlers, and at the entrance to a plane’s cargo hold.

The system could be used not only to track down misplaced bags but also prevent them from getting lost in the first place by making sure that a bag bound for San Francisco doesn’t get misdirected to a flight headed for Dallas.

Passengers may even be able to track the progress of their own luggage via e-mail or the electronic check-in kiosks the airline operates in the airport.

Henry Harteveldt, principal travel analyst with Forrester Research in Cambridge, said he didn’t think RFID would give Delta a marketing edge in distinguishing itself from its competitors.

“I don’t think a customer will choose Delta because of this,” Harteveldt said. “But if it can help Delta reduce some of the $100 million it spends each year on lost luggage and retrieval. That’s where it really starts to have meaning. This is a business improvement process, as opposed to a major enhancement in customer service.”

Michael J. Liard, RFID program director at Venture Development Corp. in Natick, estimated the chips Delta will be using will cost about $20 to 30 cents each.

The price should come down, he said, as more companies adopt RFID technology.

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More Recently

AUTO-ID LABS at MIT TO RESEARCH RFID TECHNOLOGY FOR HEALTHCARE

• Provide objective, coordinated and comprehensive body of research

• Application of automated identification, mass serialization, networking and sensing technology to Healthcare.

• Foundation of research for organizations to make sound decisions during the deployment of Auto-ID infrastructure for both current and future applications.

• In a separate exercise, the HCRI will also coordinate physical trials to validate its research
Factory to Factory Integration

By: Dave Huntley – Kinesys Software

Abstract:
This will introduce the technologies that are expected to be used for exchanging E142 data between factories. First of the E142.3 Web Services (SEMI #4068) will be discussed and then the integration between E142 and RosettaNet.

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Factory to Factory Integration

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Secure Transfer

- No lost maps!
- Fast transfer
- Sensitive data encrypted
- Non-repudiation
  - Sender and receiver can prove transaction occurred
Integration with RosettaNet

• RosettaNet TF
  – 7C7 PIP “Notify of Semiconductor Test Data” published July 2004
  – Based on XML Schemas
  – Different scope from SEMI E142
  – Will initiate joint activity with SEMI Sort Map TF in July 2005 at Semicon West

• SEMI Sort Map TF
  – Submit SNARF after July 2005 at Semicon West to integrate E142 into the 7C7 PIP Schema
  – Requirement: Test and Assembly foundries must be able to use E142 with or without RosettaNet
Plant to Plant Integration
Business to Business Integration
Test Data Feedback

- Rebuild wafer maps from final test
- Connect final test to inspection & test in wafer fab
- Identify process problems
- Improve yield
- Provide instant device tracking reports