Outline

- Problems caused by static charge
- Static Control Basics – Grounding and Ionization
- Static control requirements – Semiconductor Industry Standards
  - SEMI E78 – Static control in Production Equipment
  - SEMI E129 – Controlling Static Charge in the Factory
  - International Technology Roadmap for Semiconductors
  - ANSI ESD S20.20 – Static Control Program
- Conclusions
Static Charge Problems
Contamination and ESD

Static Charge

Yield
Throughput

Disk Media
Wafers
FPD Screens

MR Heads
Reticles
Integrated Circuits

Equipment

Contamination
ESD Damage
Process Interruptions
Contamination Study

200 mm wafer in a Class 1 Mini-Environment

- **Wafer at 0 V**
  - class 1 mini environment for 6 weeks

- **Wafer at 2000 V**
  - class 1 mini environment for 6 weeks
Electrostatic Discharge (ESD) Responsible For Many Unidentified Failures

- Quality Issues – Catastrophic ESD failures occur at the wafer level, the device level, the board level and the equipment level. ESD also damages film, medical devices, and optics.

- Reliability Issues - ESD can cause latent defects that may develop into failures at a future date.

- The cost of an ESD failure increases as a device evolves from a die on a wafer into a component within a system.
Damage Caused by Electrostatic Discharge (ESD)

1.5 μm
ESD Generates Radio Waves That Affect Microprocessors

Equipment structures and control cables make excellent antennas

- Scrambled Program Instructions and Data
- Microprocessor Lockup
- “Software Errors”
The Basics

- Static Charge Generation
  - Triboelectric Charging
  - Induction Charging

- Static Charge Control
  - Personnel Grounding
  - Worksurface Grounding
  - Static Dissipative Materials

- Insulators
Insulators vs. Conductors

- The generation and storage of electrostatic charge occurs primarily on **insulators** and **isolated conductors**. These materials are used throughout the work environment.

- Conventional grounding techniques cannot remove charges from insulators.

- There are two passive methods for removing charges from insulators:
  1) Surface treatments to attract moisture to the surface.
  2) Relative Humidity in excess of 40%.

- The third option is to make the air more conductive by ionizing it.
Neutralizing Static Charge with Bipolar Air Ionization
International Technology Roadmap for Semiconductors (ITRS) 2005

Factory Integration Chapter

Static Control – pg 35
download - www.sematech.org
Technical Requirements - Electrostatics

### Notes for Tables - Static Charge Limits

1. Facility surface electric field limits apply on all components of the factory, including construction materials, furniture, people, equipment, and carriers.
2. Wafer and photomask surface electric fields measured when they are removed from their carriers.
3. Static charge on devices measured when they are removed from their carriers.
4. For measurement techniques, refer to SEMI E78 or SEMI E43.
5. Measurements in V/cm are made with an electrostatic fieldmeter at 2.5cm (one inch).
6. Measurements in nC are made using a Faraday Cup or coulombmeter.
7. Preventing ESD damage requires an understanding of individual device and process sensitivities to ESD. These will need to be established by appropriate testing. Specific devices may require lower limits than those contained in the table.
8. Levels in volts (V) are equivalent device voltages assuming a 10pF device capacitance.

For 2005 – 90 volts/cm and 0.8 nanocoulombs
For 2020 – 15 volts/cm and 0.024 nanocoulombs
SEMI E78-0706

Guide to Assess and Control Electrostatic Discharge (ESD) and Electrostatic Attraction (ESA) for Equipment
Why? – Static charge continues to be a problem throughout silicon, reticle, and device manufacturing facilities, not just in the equipment.
# SEMI E78 and E129

## Recommended Electrostatic Limits

<table>
<thead>
<tr>
<th>Year Node</th>
<th>Electrostatic Discharge, nC</th>
<th>Electrostatic Field, V/cm</th>
<th>V/inch</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000 180 nm</td>
<td>2.5–10</td>
<td>200</td>
<td>500</td>
</tr>
<tr>
<td>2002 130 nm</td>
<td>2.0</td>
<td>150</td>
<td>375</td>
</tr>
<tr>
<td>2003 100 nm</td>
<td>1.5</td>
<td>125</td>
<td>300</td>
</tr>
<tr>
<td>2004 90 nm</td>
<td>1.0 (100 volts on a 10 pf device)</td>
<td>100</td>
<td>250</td>
</tr>
<tr>
<td>2006 70 nm</td>
<td>0.6</td>
<td>80</td>
<td>200</td>
</tr>
<tr>
<td>2007 65 nm</td>
<td>0.5</td>
<td>70</td>
<td>175</td>
</tr>
<tr>
<td>2009 50 nm</td>
<td>0.3</td>
<td>55</td>
<td>140</td>
</tr>
<tr>
<td>2010 45 nm</td>
<td>0.25</td>
<td>50</td>
<td>125</td>
</tr>
<tr>
<td>2013 32 nm</td>
<td>0.125</td>
<td>35</td>
<td>88</td>
</tr>
<tr>
<td>2015 25 nm</td>
<td>0.08</td>
<td>28</td>
<td>70</td>
</tr>
<tr>
<td>2018 18 nm</td>
<td>0.04</td>
<td>20</td>
<td>50</td>
</tr>
</tbody>
</table>
ESD Task Force
Issues for Future Discussion

- Relationship to the ITRS
  - Technology Node designations
  - DRAM vs. Microprocessor table values
  - Random faults per mask level vs. PWP used in allowable electric field calculations
  - DRAM ½ pitch vs. MPU/ASIC ½ pitch vs. MPU/ASIC Metal 1 ½ pitch

- Different charge levels for devices, wafers, and reticles (10pf for devices, 220pf for wafers, 70-100pf for photomasks)

- Scale electric field limits for particle deposition based on killer particle size. Now they are mostly based on protecting reticles.

- E78 - Review and/or remove the “background information” in many of the sections and include in an Appendix/Related Information section.

- E78 - Write clear instructions on the use of Table 1 in Section 12. (see 4 step process in Comment KT-3)

- E78 - Rewrite Section 9 to include details on type(s) of tests, number and type(s) of samples, etc. to avoid supplier/user negotiations over test methodology

- E129 – Differentiate between requirements for areas where devices and reticles are handled, and those areas where they are not present. In/outside FOUPs and reticle carriers, minienvironments, equipment, etc.

- Reticle electrostatic field issues.
ANSI ESD S20.20

Standard for the Development of an Electrostatic Control Program for the Protection of Electrical and Electronic Parts, Assemblies and Equipment (for 100 volt HBM sensitive devices)

Free Download from ESD Association
www.esda.org

Available in Chinese and Spanish
S20.20 Program Requirement for 100 volt Human Body Model Devices

- Ground everything that is conductive or static dissipative.
- Keep charged insulators and isolated conductors 30 cm away from sensitive product at all times.
- Use ionization whenever there are process essential insulators in the product or process.
- Establish facility audit and training programs.
# Cost of "Discovery"

<table>
<thead>
<tr>
<th>Activity</th>
<th>Associated Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>Problem Occurs</td>
<td>Product Losses</td>
</tr>
<tr>
<td>Investigation of Cause</td>
<td>Engineering Time, Analysis Costs, Product Losses</td>
</tr>
<tr>
<td>Development and Testing of Trial Solutions</td>
<td>Engineering Time, Trial Solution Cost, Product Losses</td>
</tr>
<tr>
<td>Installation of Chosen Solution</td>
<td>Solution Cost, Product Losses</td>
</tr>
</tbody>
</table>

*The cost of discovery is 10-100 times the cost of the solution!*

Prevent static problems – It’s too costly to solve them
Semiconductor Issue
Field-Induced CDM

- Any charged object is a potential hazard
- Static fields cause ESD damage when a conductor is grounded in the field - devices
- Changing electric fields from a discharge or movement can cause ESD damage without grounding - reticles
- Isolate by distance (field drops as $1/distance^2$)
- Neutralize the charge
Field Induced CDM Without Grounding
Reticle Damage Caused By ESD
New Customer Requirements

- Documented Static Control Program
- Maintain Static Levels in the whole factory less than 100 volts
  - ANSI ESD S20.20 – 100 volts HBM
  - SEMI E129 – 100 volts CDM for a 10 pf IC (1 nC)
  - ITRS for 2004 – 100 volts CDM for a 10 pf IC (1 nC)
- Required for New Business
Achieving the 100 volt Customer Requirement

- Ground all conductors - 0 volts
- Reduce the charge on insulators and isolated conductors with ionizers – less than 100 volts/inch
- **Educate the customer** – 100 volts/inch on a Fieldmeter has nothing to do with a 100 volt device ESD sensitivity
Conclusions

- Static charge issues will not go away. Solving them becomes more important with technology change.

- A complete static control program requires grounding, proper material selection, and ionization to control charge on insulators. Use ANSI ESD S20.20.

- SEMI E78 and E129 address static control requirements for the semiconductor factory of the future, synchronizing with ITRS 2005. These documents will be harmonized and updated every 2 years.

- The discussion of the many issues concerning static charge control in semiconductors is continuing. Please join the ESD Task Force to be part of that discussion.

- Next meeting Tuesday October 17 1:30-4:30PM

Static control is not an option!