Overview of Electrostatic Recommendations in Updated E78, E129, and ITRS 2005

Arnold Steinman M.S.E.E.

Chief Applied Technologist

MKS, Ion Systems

Leader – SEMI ESD Task Force

ESDA Certified ESD Program Manager

NARTE Certified ESD Engineer

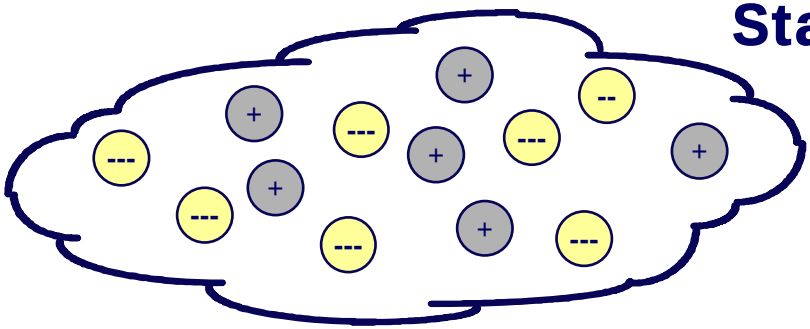
asteinman@ion.com

mks
Technology for Productivity
Ion Systems

Outline

- Problems caused by static charge
- Static Control Basics – Grounding and Ionization
- Static control requirements – Semiconductor Industry Standards
  - SEMI E78 – Static control in Production Equipment
  - SEMI E129 – Controlling Static Charge in the Factory
  - International Technology Roadmap for Semiconductors
- ANSI ESD S20.20 – Static Control Program
- Conclusions

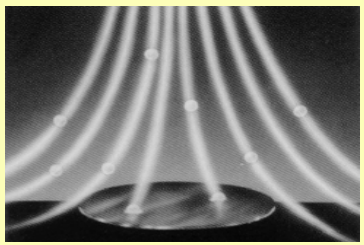
Static Charge Problems Contamination and ESD



Yield **Throughput**

Disk Media **Wafers**

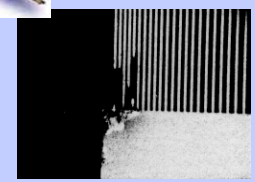
FPD Screens



Contamination

MR Heads

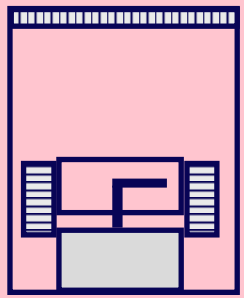
Reticles



Integrated Circuits

ESD Damage

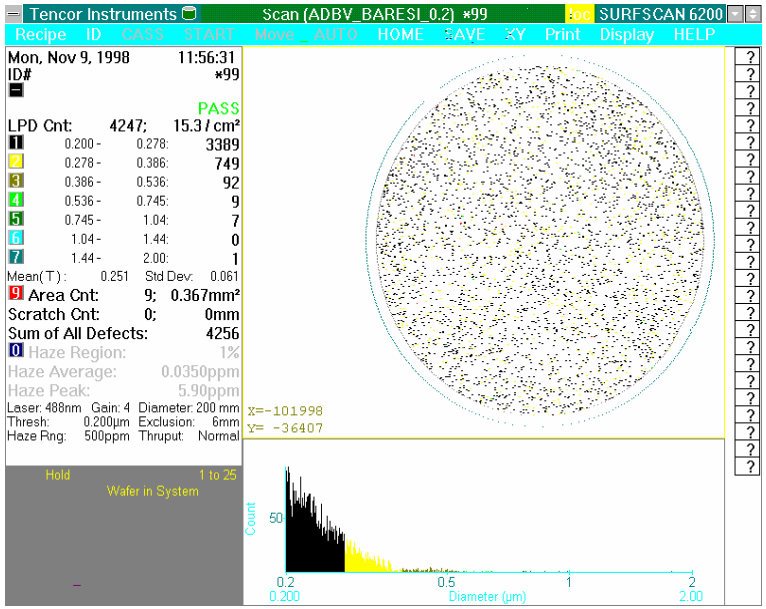
Equipment

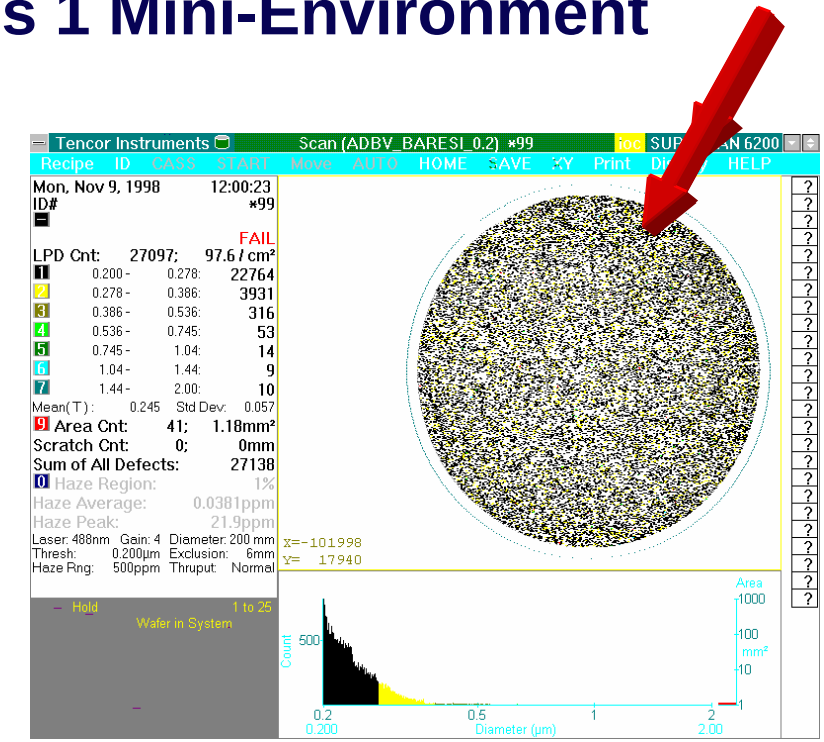


Process Interruptions

Contamination Study

200 mm wafer in a Class 1 Mini-Environment



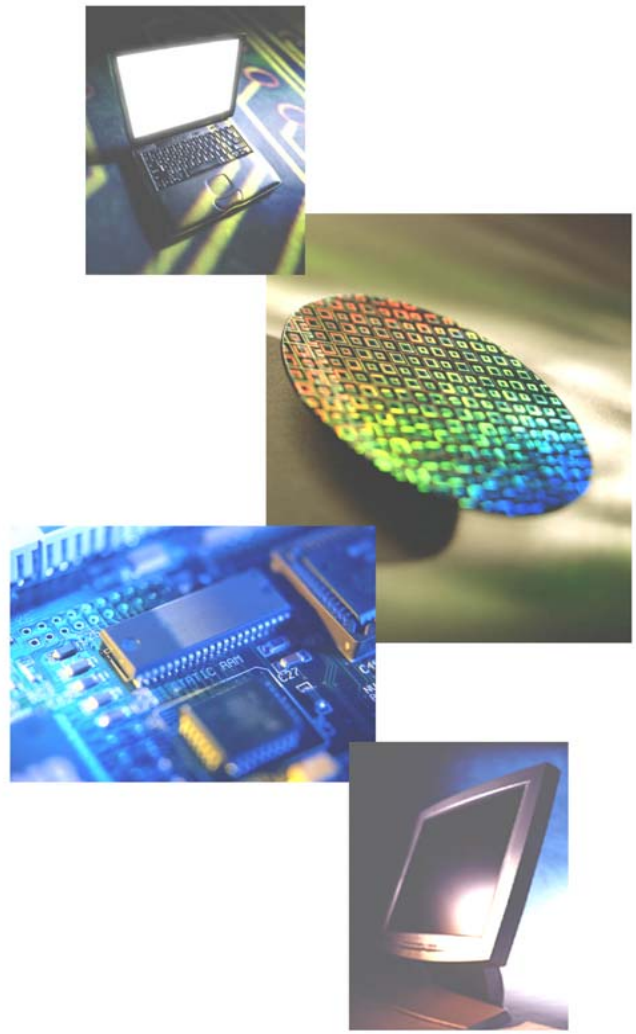


Wafer at 0 V
class 1 mini environment for 6 weeks

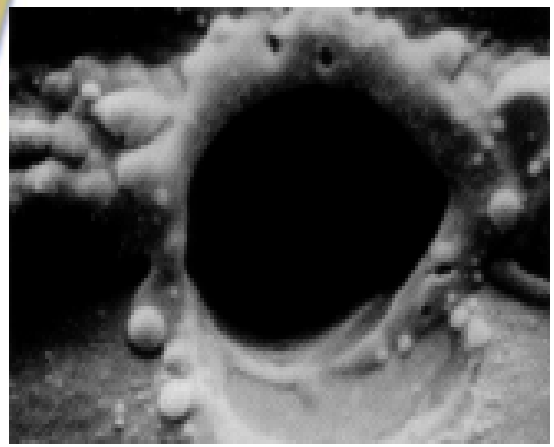
Wafer at 2000 V
class 1 mini environment for 6 weeks

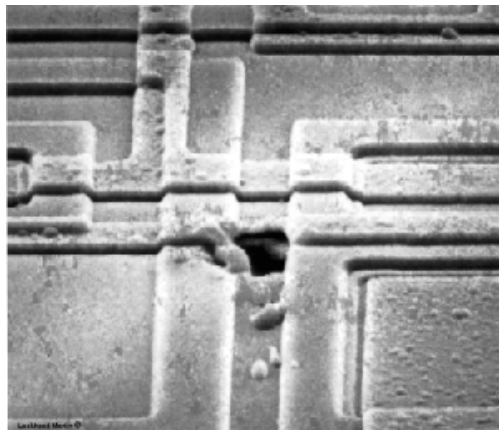
Electrostatic Discharge (ESD) Responsible For Many Unidentified Failures

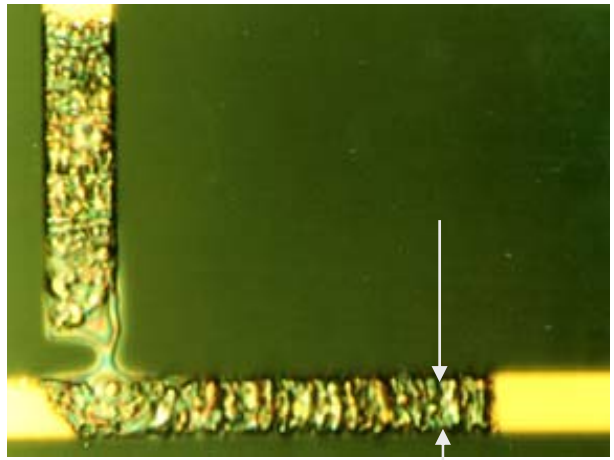
- **Quality Issues – Catastrophic ESD failures occur at the wafer level, the device level, the board level and the equipment level. ESD also damages film, medical devices, and optics.**
- **Reliability Issues - ESD can cause latent defects that may develop into failures at a future date.**
- **The cost of an ESD failure increases as a device evolves from a die on a wafer into a component within a system.**



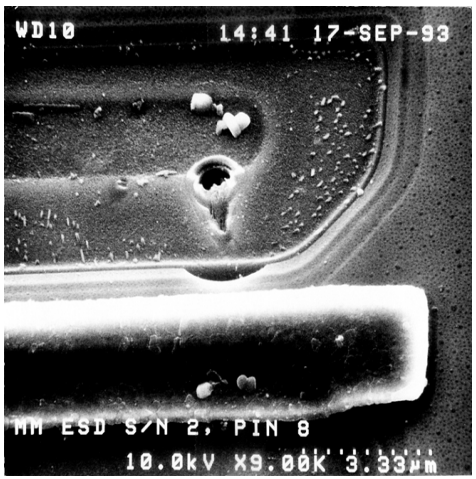
Damage Caused by Electrostatic Discharge (ESD)

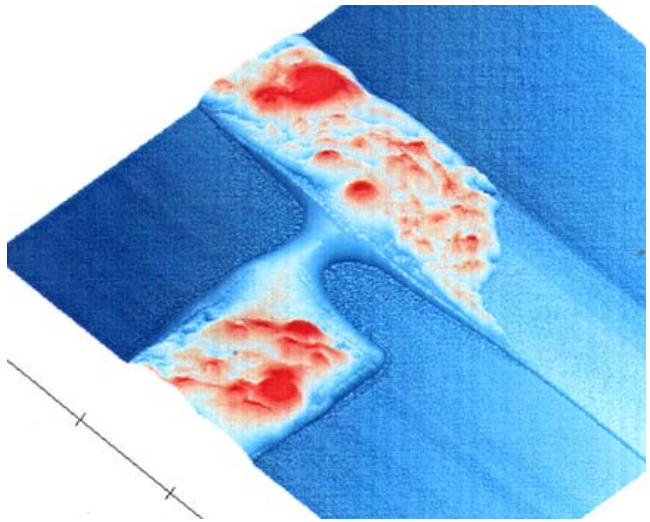






1.5 μm





ESD Generates Radio Waves That Affect Microprocessors

Equipment structures and control cables make excellent antennas

- **Scrambled Program Instructions and Data**
- **Microprocessor Lockup**
- **“Software Errors”**

The Basics

- Static Charge Generation
  - Triboelectric Charging
  - Induction Charging
- Static Charge Control
  - Personnel Grounding
  - Worksurface Grounding
  - Static Dissipative Materials
- Insulators

Insulators vs. Conductors

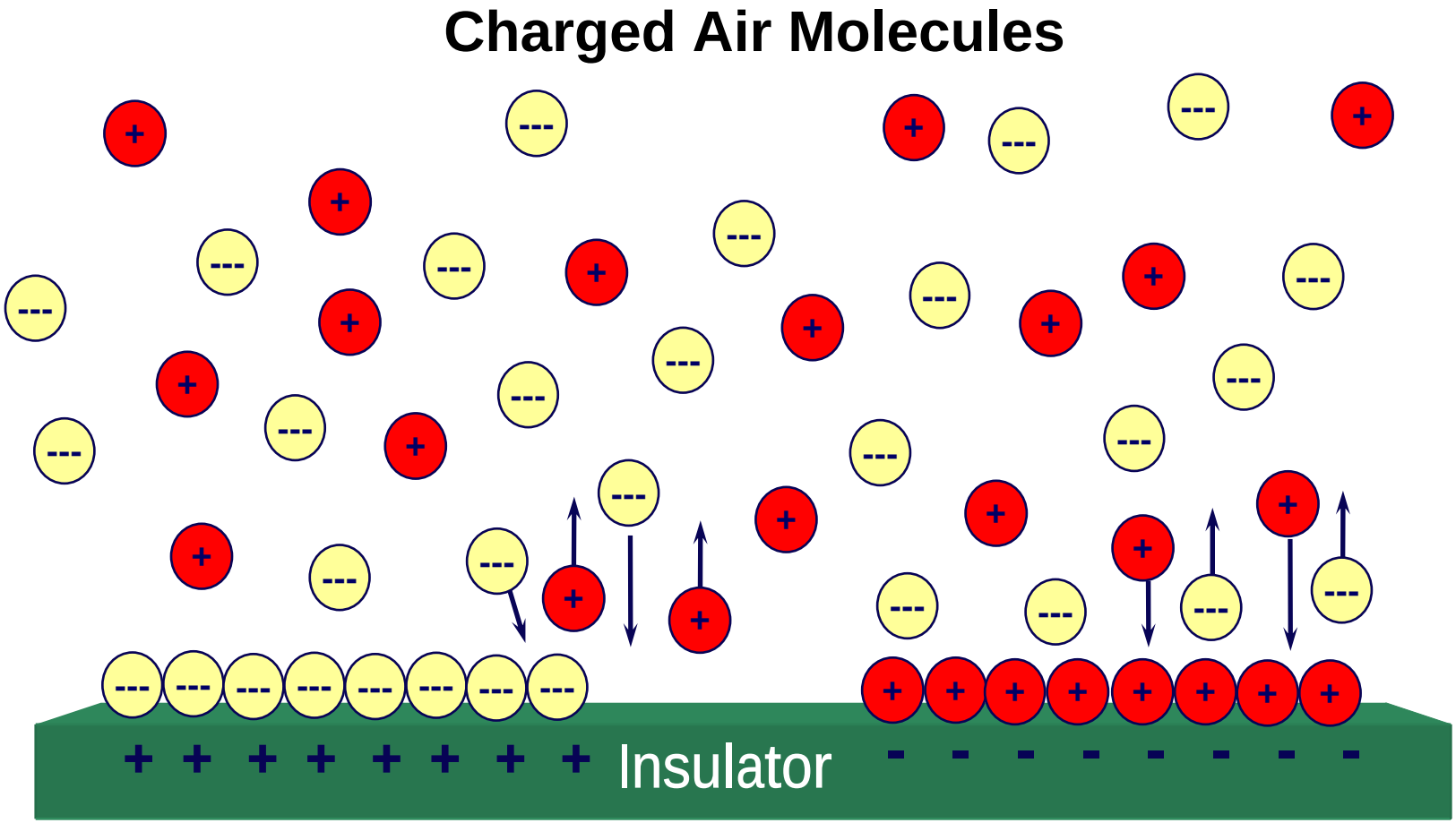
- **The generation and storage of electrostatic charge occurs primarily on insulators and isolated conductors. These materials are used throughout the work environment.**

- **Conventional grounding techniques cannot remove charges from insulators.**

- **There are two passive methods for removing charges from insulators:**
  1) **Surface treatments to attract moisture to the surface.**
  2) **Relative Humidity in excess of 40%.**

- **The third option is to make the air more conductive by ionizing it.**

Neutralizing Static Charge with Bipolar Air Ionization



International Technology Roadmap for Semiconductors (ITRS) 2005

Factory Integration Chapter

Static Control – pg 35

download - www.sematech.org

Technical Requirements - Electrostatics

Year Technology Node	2004 90nm	2005 80nm	2006 70nm	2007 65nm	2008 57nm	2009 50nm	2010 45nm	2011 40nm	2012 35nm	2013 32nm	2014 28nm	2015 25nm	2016 22nm	2017 20nm	2018 18nm	2019 16nm	2020 14nm
Maximum allowable electrostatic field on facility surfaces	100 V/cm	90 V/cm	80 V/cm	70 V/cm	63 V/cm	55 V/cm	50 V/cm	44 V/cm	38 V/cm	35 V/cm	31 V/cm	28 V/cm	25 V/cm	22 V/cm	20 V/cm	18 V/cm	15 V/cm
Maximum allowable static charge on devices	1.0 nC (100V)	0.8 nC (80V)	0.60 nC (60V)	0.5 nC (50V)	0.40 nC (40V)	0.30 nC (30V)	0.25 nC (25V)	0.20 nC (20V)	0.15 nC (15V)	0.125 nC (12.5V)	0.10 nC (10V)	0.08 nC (8V)	0.06 nC (6V)	0.05 nC (5V)	0.04 nC (4V)	0.03 nC (3V)	0.025 nC (2.5V)
Maximum allowable electrostatic field on wafer and photomask surfaces	100 V/cm	90 V/cm	80 V/cm	70 V/cm	63 V/cm	55 V/cm	50 V/cm	44 V/cm	38 V/cm	35 V/cm	31 V/cm	28 V/cm	25 V/cm	22 V/cm	20 V/cm	18 V/cm	15 V/cm

Notes for Tables - Static Charge Limits

1. Facility surface electric field limits apply on all components of the factory, including construction materials, furniture, people, equipment, and carriers.
2. Wafer and photomask surface electric fields measured when they are removed from their carriers.
3. Static charge on devices measured when they are removed from their carriers.
4. For measurement techniques, refer to SEMI E78 or SEMI E43.
5. Measurements in V/cm are made with an electrostatic fieldmeter at 2.5cm (one inch).
6. Measurements in nC are made using a Faraday Cup or coulombmeter.
7. Preventing ESD damage requires an understanding of individual device and process sensitivities to ESD. These will need to be established by appropriate testing. Specific devices may require lower limits than those contained in the table.
8. Levels in volts (V) are equivalent device voltages assuming a 10pF device capacitance.

For 2005 – 90 volts/cm and 0.8 nanocoulombs

For 2020 – 15 volts/cm and 0.024 nanocoulombs

SEMI E78-0706

SEMI E78-0706
Guide to Assess and Control Electrostatic Discharge (ESD) and Electrostatic Attraction (ESA) for Equipment

SEMI E78-0998
ELECTROSTATIC COMPATIBILITY - GUIDE TO ASSESS AND CONTROL ELECTROSTATIC DISCHARGE (ESD) AND ELECTROSTATIC ATTRACTION (ESA) FOR EQUIPMENT

1 Purpose

1.1 The purpose of this document is to minimize the negative impact on productivity caused by static charge in semiconductor manufacturing environments. It is a guide for establishing electrostatic compatibility of equipment used in semiconductor manufacturing.

1.2 Electrostatic surface charge causes a number of undesirable effects in semiconductor manufacturing environments. Electrostatic discharge (ESD) damages both products and reticles. ESD events also cause electromagnetic interference (EMI), resulting in equipment malfunctions. Charged wafer and reticle surfaces attract particles (electrostatic attraction or ESA) and increase the defect rate. Charge on products can also result in equipment malfunction or product breakage. Operating problems and additional product defects due to static charge can have a negative impact on the cost of ownership of semiconductor manufacturing equipment (refer to SEMI E35).

1.3 An increasing amount of semiconductor production is done in minienvironments or within the production equipment. The majority of static related problems occur while the product is in its carriers, or being transferred from them, by the production equipment.

1.4 Static control methods can be incorporated in the equipment design to reduce static charge to acceptable levels. This guide will be used primarily by equipment manufacturers during the design of their equipment. There are test methods available (see Sections 6 and 7 of this guide) to demonstrate the effectiveness of the static control methods. The end user will be able to use the same test methods to verify compliance with an equipment purchase specification.

2 Scope

2.1 The scope of this document is limited to methods of measurement and a guide for the maximum recommended level of static charge on:

— Product or reticles
— Carriers
— Parts of the input/exit ports of equipment and minienvironments

2.2 This document presents a matrix of maximum recommended levels of static charge on products, reticles, carriers, and the input and exit ports of production equipment or minienvironments. The purpose is to:

— Reduce product, reticle, and equipment damage due to ESD
— Reduce equipment lock-up problems due to ESD events.
— Reduce the attraction of particles to charged surfaces.

2.3 This document references SEMI E43 and other methods of measuring static charge. Related Information 1 of this document contains a theoretical investigation of electrostatic particle attraction, as well as case histories from users and equipment manufacturers as to the static charge problems encountered and how they were solved. A bibliography of related technical papers is also included. Related Information 2 describes static control methods commonly used in semiconductor manufacturing.

3 Limitations

3.1 *Static Measurements* — Measurements of electrostatic quantities such as charge, electric field, and voltage are difficult to make. The nature of the object (insulator or conductor), its geometry, its surroundings, and the measuring equipment itself, are only a few of the factors affecting the accuracy of an electrostatic measurement.

3.1.1 Similarly, it is difficult to relate the measurement of an electrostatic quantity to its effect on products or equipment. For example, an ESD simulator produces a standardized discharge waveform when a capacitor is discharged at a known voltage. This device is used to establish the ESD damage threshold for semiconductor products, or the effect of ESD on equipment. While the amount of charge transferred is known ($q = CV$), the maximum current that results is not. There is no guarantee that the same amount of charge would produce

1 SEMI E78-0998 © SEMI 1998

SEMI E129-0706

Guide to Assess and Control Electrostatic Charge in a Semiconductor Manufacturing Facility

SEMI E78-0998

ELECTROSTATIC COMPATIBILITY - GUIDE TO ASSESS AND CONTROL ELECTROSTATIC DISCHARGE (ESD) AND ELECTROSTATIC ATTRACTION (ESA) FOR EQUIPMENT

1 Purpose

2 Scope

3 Limitations

Why? – Static charge continues to be a problem throughout silicon, reticle, and device manufacturing facilities, not just in the equipment.

SEMI E78 and E129 Recommended Electrostatic Limits

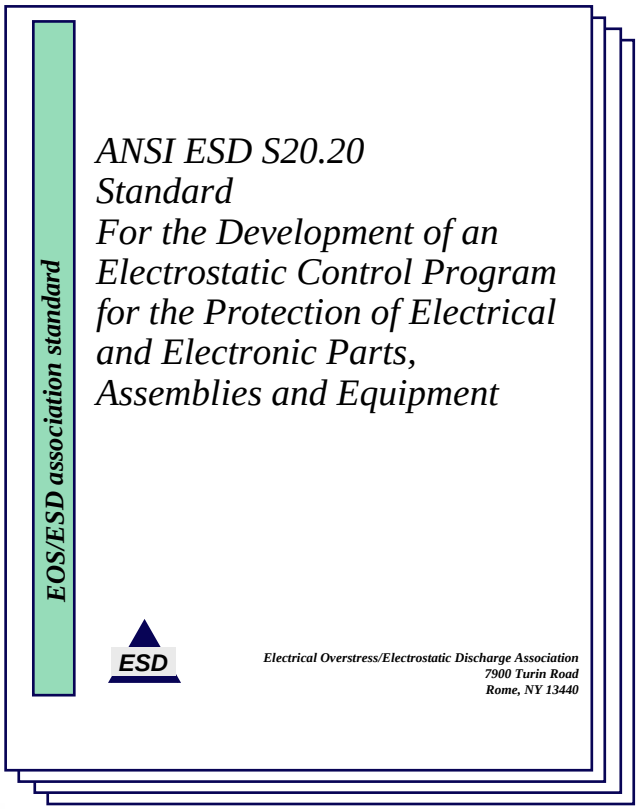
Year Node	*Electrostatic Discharge, nC*	*Electrostatic Field, V/cm*	*V/inch*
2000 180 nm	2.5–10	200	500
2002 130 nm	2.0	150	375
2003 100 nm	1.5	125	300
2004 90 nm	1.0 (100 volts on a 10 pf device)	100	250
2006 70 nm	0.6	80	200
2007 65 nm	0.5	70	175
2009 50 nm	0.3	55	140
2010 45 nm	0.25	50	125
2013 32 nm	0.125	35	88
2015 25 nm	0.08	28	70
2018 18 nm	0.04	20	50

ESD Task Force
Issues for Future Discussion

- Relationship to the ITRS
  - Technology Node designations
  - DRAM vs. Microprocessor table values
  - Random faults per mask level vs. PWP used in allowable electric field calculations
  - DRAM ½ pitch vs. MPU/ASIC ½ pitch vs. MPU/ASIC Metal 1 ½ pitch
- Different charge levels for devices, wafers, and reticles (10pf for devices, 220pf for wafers, 70-100pf for photomasks
- Scale electric field limits for particle deposition based on killer particle size. Now they are mostly based on protecting reticles.
- E78 - Review and/or remove the “background information” in many of the sections and include in an Appendix/Related Information section.
- E78 - Write clear instructions on the use of Table 1 in Section 12. (see 4 step process in Comment KT-3)
- E78 - Rewrite Section 9 to include details on type(s) of tests, number and type(s) of samples, etc. to avoid supplier/user negotiations over test methodology
- E129 – Differentiate between requirements for areas where devices and reticles are handled, and those areas where they are not present. In/outside FOUPs and reticle carriers, minienvironments, equipment, etc.
- Reticle electrostatic field issues.

ANSI ESD S20.20

International Standard



Standard for the Development of an Electrostatic Control Program for the Protection of Electrical and Electronic Parts, Assemblies and Equipment (for 100 volt HBM sensitive devices)

Free Download from ESD Association www.esda.org

Available in Chinese and Spanish

S20.20 Program Requirement for 100 volt Human Body Model Devices

- **Ground everything that is conductive or static dissipative.**
- **Keep charged insulators and isolated conductors 30 cm away from sensitive product at all times**
- **Use ionization whenever there are process essential insulators in the product or process**
- **Establish facility audit and training programs**

Cost of "Discovery"

Activity	Associated Cost
Problem Occurs	Product Losses
Investigation of Cause	Engineering Time Analysis Costs Product Losses
Development and Testing of Trial Solutions	Engineering Time Trial Solution Cost Product Losses
Installation of Chosen Solution	Solution Cost Product Losses

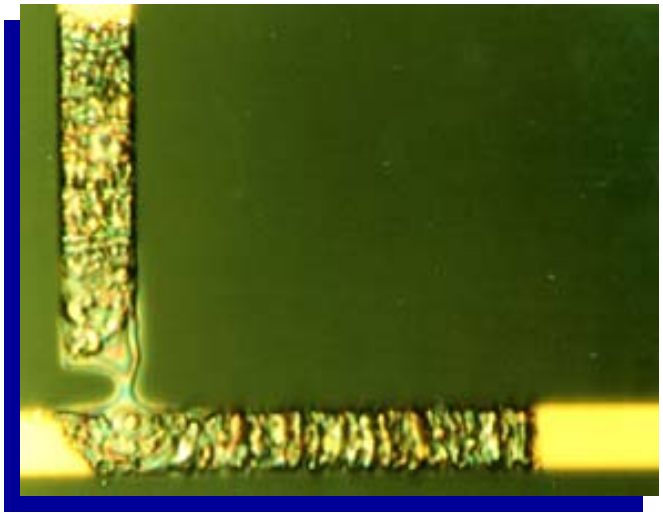
The cost of discovery is 10-100 times the cost of the solution!

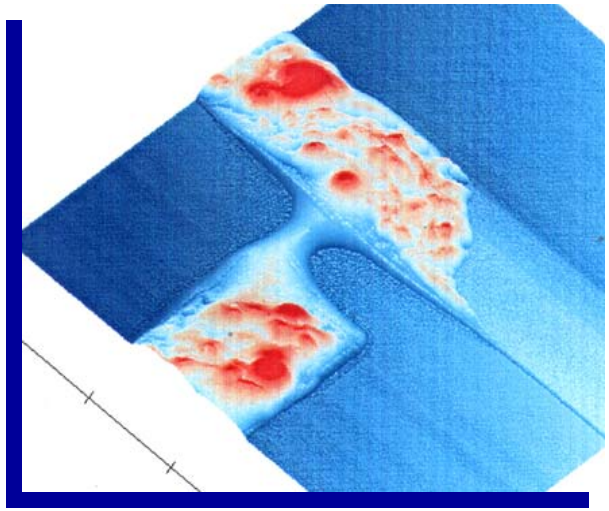
Prevent static problems – It's too costly to solve them

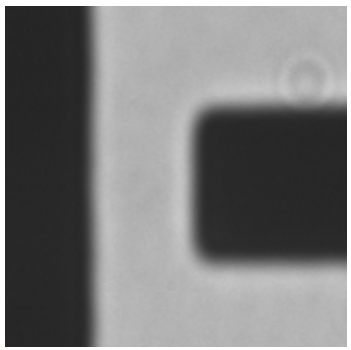
Semiconductor Issue Field-Induced CDM

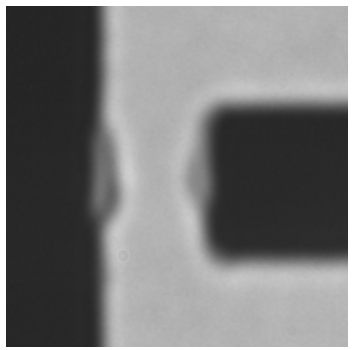
- Any charged object is a potential hazard
- Static fields cause ESD damage when a conductor is grounded in the field - devices
- Changing electric fields from a discharge or movement can cause ESD damage without grounding - reticles
- Isolate by distance (field drops as $1/\text{distance}^2$)
- Neutralize the charge

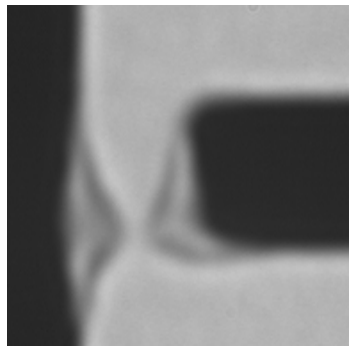
Field Induced CDM Without Grounding Reticle Damage Caused By ESD

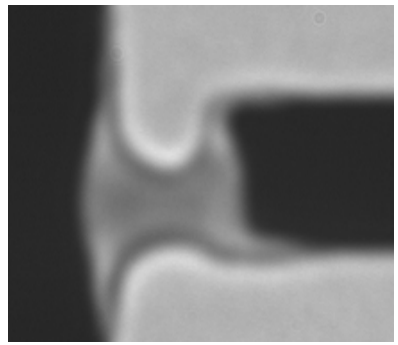












New Customer Requirements

- Documented Static Control Program
- Maintain Static Levels in the whole factory less than 100 volts
  - ANSI ESD S20.20 – 100 volts HBM
  - SEMI E129 – 100 volts CDM for a 10 pf IC (1 nC)
  - ITRS for 2004 – 100 volts CDM for a 10 pf IC (1 nC)
- Required for New Business

Achieving the 100 volt Customer Requirement

- **Ground all conductors - 0 volts**
- **Reduce the charge on insulators and isolated conductors with ionizers – less than 100 volts/inch**
- **Educate the customer – 100 volts/inch on a Fieldmeter has nothing to do with a 100 volt device ESD sensitivity**

Conclusions

- Static charge issues will not go away. Solving them becomes more important with technology change.
- A complete static control program requires grounding, proper material selection, and ionization to control charge on insulators. Use ANSI ESD S20.20.
- SEMI E78 and E129 address static control requirements for the semiconductor factory of the future, synchronizing with ITRS 2005. These documents will be harmonized and updated every 2 years
- The discussion of the many issues concerning static charge control in semiconductors is continuing. Please join the ESD Task Force to be part of that discussion.
- Next meeting Tuesday October 17 1:30-4:30PM

Static control is not an option!